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Projekt.	Kovačevič		Znak						
Pregled.	Rogač		Št. obv.	11-017					
Števil.	J. Bojanić		Datum	17.12.86					
Stand.			Podpis						

Iskra Delta
proizvodnja računalniških sistemov in inženiring, p.o.

Naziv	List	Stran	J	K	Identifikacijska številka
TECHNICAL MANUAL	1				33837044

Namembnost kopije	Arhiv	Merilo	Sekcija	Namesto identifikacijske številke
				22067044

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VME MODULE

VME-CPU 286

TEHNICAL MANUAL

FIRST EDITION: SEPTEMBER 1986

CONTENTS
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1. GENERAL INFORMATION

The VME CPU 286 is a highly integrated board having the features of a single board computer since it incorporates the local memory of RAM type, local memory of EPROM type, input/output capabilities, time functions, interrupt controller, and interface for the VME bus.

The board uses highly capable CPU, intergrated circuit Intel 80286-8 together with the numerical coprocessor 80287-6.

The synthesis of the 80286 microprocessor and the VME bus represents a rare combination on the VME market, since it offers a central processing unit of high performance and wide application for any professional applications where a high level of operation reliability is required. The central processing unit would be of a special interest for office automation applications where IBM PC/XT/AT play a significant role.

The board is also extremely useful and highly appropriate as a central processing unit for the building of engineering workstations regarding strong HW support for numerical operations being supported by all SW system packages available at the moment (OS, compilers, libraries).

Taking into consideration the architecture of microprocessor 80286 and on-chip integrated memory management unit the board can be used in building of multiuser and multitasking systems as well as for the implementation of the high performance operating systems of UNIX type.

2. FEATURES

8 MHz INTEL 80286 CPU
5 MHz INTEL 80287 Numerical coprocessor
80 bit IEEE 754 compatible
On-chip memory management
Four level protection
1 Gb virtual address space
16 Mb physical address space
Separate instruction stack and data space
VME bus compatible
Option DTB master: A24.D16
Option DTB slave: A24.D16
Option BTO (bus time out)
Option ONE level arbiter
Option ROR, RWD requester
Interrupt handler for five IRQ lines
On-board memory
128, 256 or 512 KB dynamic RAM
with almost no wait states
Real time clock
seconds, minutes, hours, days, months, years, alarm,
periodic interrupt
Two bootstrap EPROM sockets for up to 64 KB
Two RS232C serial communication ports
synchronous or asynchronous
Bus lock support for multiprocessor configuration (Rev. D)

3. DESCRIPTION

The VME 286 offers a powerful combination of the latest, high performance technology and standards: the richess and portability of XENIX (UNIX) and 16/32 bit VME bus for multi-vendor support and wide availability of products.

The VME 286 is a 16 bit high performance CPU for the use in the VME bus systems. It is based on the powerful INTEL 80286 microprocessor and 80287 numerical coprocessor. The 80286's pipelined architecture and 16 MHz frequency offer a level of performance comparable to that of many high-end minicomputers. Large virtual address space and 286 hardware enforced data protection make it especially suitable for the demanding multitasking applications.

Over 120 manufacturers offer more than 800 VME bus based hardware and software products with the VME bus being formally standardized for the world wide use by both the IEEE and IEC. The VME's 286 high performance, capability to run both XENIX and MS DOS operating systems with a huge base of existing software and leading 16/32 standard bus offers a unique "OPEN ARCHITECTURE", performance, reliability and future expansion while preserving the software investment and reducing the product development cycle.

VME bus arbiter

The option ONE single level VME bus arbiter is available so that systems can be configured with the VME 286 as the VME bus controller. In that case the CPU must be physically located in VME bus slot 1 and have the arbiter jumper enabled. The arbiter controls the access to the VME bus by monitoring DTB requests on BR3* only and responding via the BG3IN*/BGOUT* daisy chain. The VME 286 itself will have the highest priority in this configuration due to its physical location in slot 1.
The VME CPU 286 board may also be used in multi processor systems or with a separate VME bus controller by the jumper disabling the arbiter and locating the card in any slot but slot 1. In this configuration the CPU will request the use of the bus via the Br3* line.

VME bus requester

Intel 80286 microprocessor requires the transfer of data through the VME bus by using the on-board VME bus requester via the BR3* line; DTB is granted via the BG3IN*/BG3OUT* daisy chain. Once the DTB has been granted, the CPU will use the bus until another request is sent (Option ROR). The VME bus requester supports the 80286 LOCK function by not releasing the bus until the cycle is terminated.

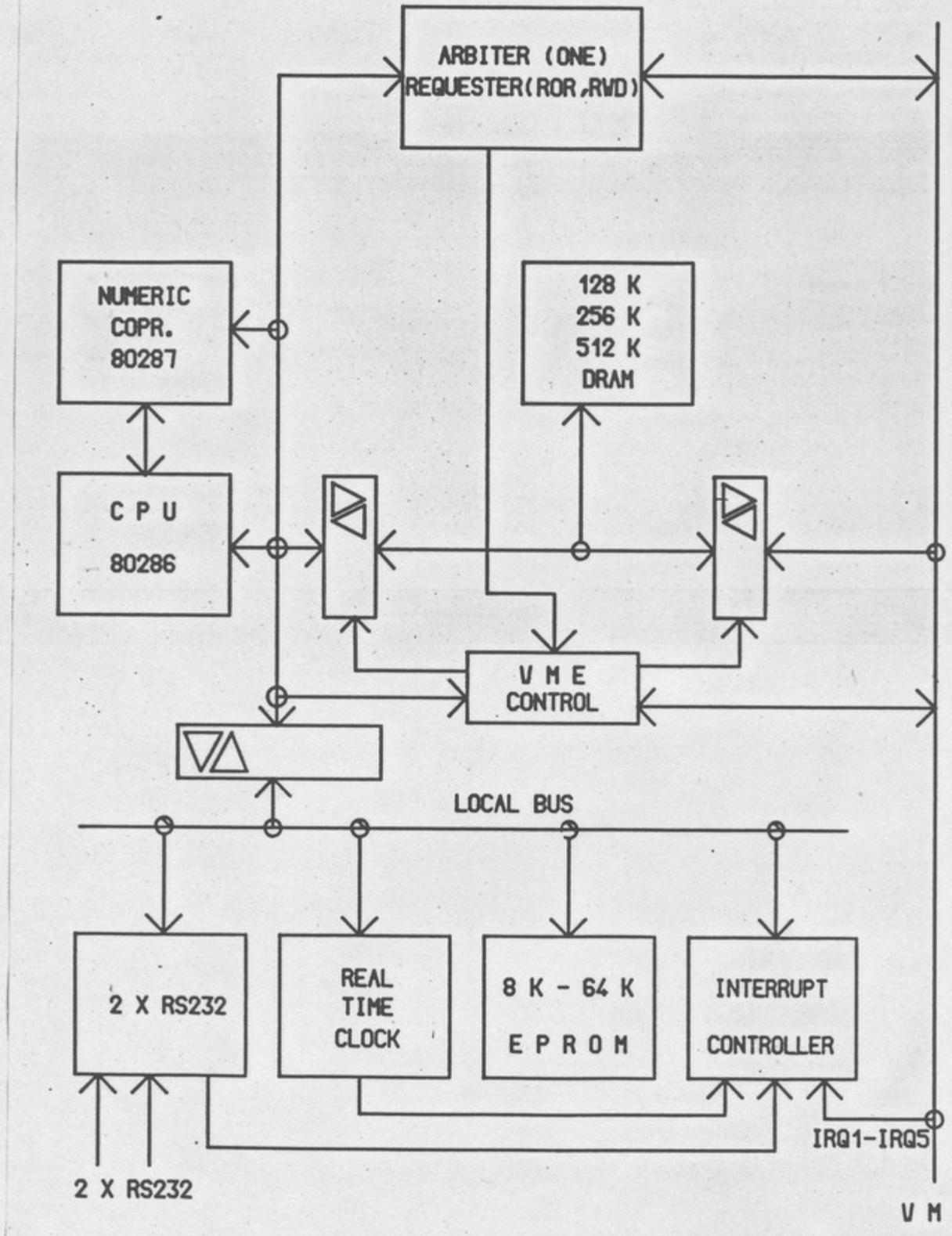


Figure 1: Triglav CPU/286 Block Diagram

Izdaja	1					List	Stran	J	K	Identifikacijska številka
Št. obvestila	11-017					8				33837044
IskraDelta proizvodnja računalniških sistemov in inženiring, p.o.						Arhiv		Namesto identifikacijske številke: 22067044		

VME bus interrupt handler

VME CPU/ 286 board uses a seven level interrupt controller. Two levels are reserved for local (on-board) interrupt processing (periodic interrupt, interrupts from serial communication controller and alarm interrupt). The remaining five levels are connected to the VME bus interrupt request lines IRQ1* - IRQ5*. Local interrupt requests are on a higher priority than VME bus interrupt requests. The status /ID byte for the VME bus interrupt requests can be generated by the interrupt handler or by the requesting device during the bus acknowledge cycle on the bus.

VME bus control functions

A special 16 MHz oscillator generates the SYSCLK signal for the use on peripheral modules. The power-up circuit generates the VME bus SYSRESET* signal and initializes the on-board circuits and the 80286 CPU upon detection +5 VDC. The manual reset on the front panel enables reinitialization of the module and the VME bus.

The bus time-out circuit monitors the execution of memory and IO cycles of the CPU and forces the conclusion of cycles not to be acknowledged. Active levels of the BERR* and ACFAIL* signals on the VME bus generate NMI as well. The source of the NMI can be determined by software from the status register.

The state of the bus SYSFAIL* signal can be read by software which is useful during the start up time to determine readiness of all modules on the bus for the normal operation.

Control and status register

The control register is used for switching from the REAL to PVAM addressing mode. It has a fixed address of F0000 (hex) in the memory address space. The setting bit 0 to logic 1 makes the on-board circuit to translate memory addresses to the PVAM mode.

The status register shows the state of the SYSFAIL* line on the bus and the source of the non-maskable interrupt (bus time-out, ACFAIL* or BERR*). The status register is an 8 bit register on address 0001 (hex) in the IO address space.

Memory management

The 80286 CPU incorporates a complete memory management unit which enables addressing of 1 MB of physical memory in the REAL mode and 16 MB of physical memory in the PVAM mode. In the PVAM mode 1 GB of the virtual memory can be addressed. The main

features of the PVAM mode are the extended physical and virtual address space, 4 level protection mechanism and special instructions for the support of the operating systems. Whenever the CPU addresses the memory or IO space which is not the local board an address space request for the VME bus is made by using the VME bus requester. During data transfer via the VME bus address modifier signals are generated by the module:

3D (hex) - standard supervisory data access
2D (hex) - short supervisory IO access (for cycles in the IO space)

When a module is in the DTB slave mode on the bus it requests the addresss modifier code 3D (hex) for the normal operation.

Real time clock

The real time clock on the VME CPU/286 board performs three functions: complete day clock with alarm, hundred year calendar, programmable periodic interrupt and square wave generator for generating periodic interrupts in conjunction with the programmable seven level interrupt controller. The circuit is built in the CMOS technology and operates at extremely low power consumption from the +5V STDBY line. Besides, it has 50 bytes of the general purpose RAM. All registers and RAM are mapped in the IO address space.

Communication controller

The communication controller has two independent 0 to 1 Mbit/sec full-duplex channels , each one with its own oscillator, baud rate generator and digital phase lock loop for discriminating clock pulses. The communication controller can operate in the asynchronous or synchronous mode supporting the SDLC/HDLC protocol.

4. OPERATION OF THE BOARD

The board consists of many fuctional modules, being separated but organised around the central processor, two local buses and the VME bus.

Microprocessor 80286 is tightly coupled with numerical coprocessor 80287 in a way which enables the operation of circuit 80287 installed in the 40 pin socket or even without it.

The central processing unit 80286 is driven by the 16 MHz or 12 Mhz clock, depending on the speed of the installed circuit (80286). The clock generator 80284 which is installed on the board has an internal 12MHz oscillator or it is driven by the external oscillator - 16 MHz viz. the SYSCLK* signal.

The generator of the clock takes care of the correct termination of each bus cycle started by the processor based on two ready signals (ARDY, SRDY) . In this way it generates the READY signal, which the processor accepts as a termination of the bus cycle. On the basis of the SRDY signal all bus cycles which access the on-board IO or memory devices are completed. On the basis of the ARDY signal all cycles are completed which access the devices on the VME bus. The clock generator 82284 takes also care of generating the appropriate RESET signal at the power up or when pressing the RESET key on the front panel.

The address decoder is connected to the address bus of the central processor. It has a task to separate the address area of the local bus, DRAM area and address area of the system bus. For each of these address areas one of the following signals is generated: CENL- (access to the local bus), RPEA- (access to the on-board memory) and LOCR (access to the system bus). There are two separated decoders for address decoding of the local bus and the on-board memory. The address area of the system bus represents the space to 16 Mb memory and 64 Kb IO address space if the mentioned address areas are excluded.The local bus is separated by the three state drivers as well as the on-board memory bus.

The central processor accepts the NMI signal (non-maskable interrupts) in case the bus cycle is not terminated in the planned time (bus time out) or in case the access to the system bus finishes with the BERR* signal (bus error) or if the ACFAIL* signal on the bus is generated.

The logic of the decoders of the address area can operate in two modes: the real mode having physical address space of max. 1 Mb and the PVAM mode having the physical address space of max.16 Mb. The logic of the decoders is set to the real mode at a power up or each reset. And it is set to the PVAM mode by the write operation into the address area of EPROM on the local bus.

4.1 LOCAL BUS

The local bus is separated from the central processor by the three state drivers. The following components are connected to the local bus:
- the EPROM memory of maximum capacity 64 Kb,
- Z8530(SCC) serial controller with two channels,
- real time clock MC 146818 (RTC)
- interrupt controller 8259A (PIC) for the local and VME bus interrupts control.

The local bus is activated when the central processing unit starts a bus cycle in the address space of the local bus viz. when the CENL signal, which selects the local bus, is activated. The CENL signal activates the local bus controller 82288, being responsible for the local bus three state drivers control and generates read and write commands for the EPROM memory or IO devices on the local bus (SCC, RTC, PIC, numerical coprocessor (NPX)). The I/O devices on the local bus are selected by the special decoder of a local bus which generates appropriate select signals for each of these devices (SCC-, RTC-, INTC-, NPX-).

A special READY logic takes care of correct termination of the cycles on the local bus where access times for different devices (RTC, SCC, PIC, NPX, EPROM) are ensured. EPROM cycles take one wait state, SCC and PIC cycles take four wait states, RTC cycles take five wait states and NPX cycles take three wait states. When reaching SCC registers it is necessary to assure cycle-to-cycle recovery time (2,2 us) under the software control.

The numerical coprocessor and the SCC clock generate a special clock generator with a basic frequency 18,432 MHz. This generator enables work of the numerical coprocessor with a frequency 6 MHz and the SCC clock with a frequency 3,072 MHz. On the basis of this SCC clock a serial transfer through both serial channels is made possible to 19200 baud and it is software settable.

4.1.1 SERIAL CHANNELS RS232C

On the VME CPU 286 board there is an integrated circuit Z8530SCC supporting two serial asynchronous or synchronour channels.

Z8530SCC drives the input/output clock 3.072 MHz which enables work up to 19200 bauds in the asynchronous mode (internal clock) and up to 1 M Baud in the synchronous mode (external clock). In the table (...) the program settable divisional constants for different speeds at different divisional factors (X1, X16, X32, X64) are shown. The channels are organised to function as DTE (Data Terminal Equipment) .
There are two jumper fields on the board where any configuration of the channels is possible. Both channels support all modem control signals (RTS, CTS, DTR, DSR, DCD, RXCLK, TXCLK).
Z8530SCC can generate the interupt request level 1 (IR1) of the 8259A interrupt controller (together with RTC interrupt). There are three types of interrupts : Transmit, Receive, and External/Status. Each interrupt type is enabled by software for both chanels through SCC control registers. Z8530SCC can place an interrupt vector (ID byte) on the local data bus if the 8259A ICW3 register bit1 is set to 1. If this bit is set to 0 than 8259A interrupt controller will place an interrupt vector (ID byte) byself for Z8530SCC interrupt request (IR1).

baud rate	X1	X16	X32	X64
50	30718	1918	958	478
75	20478	1278	638	318
150	10238	638	318	158
200	7678	478	238	118
300	5118	318	158	78
600	2558	158	78	38
1200	1278	78	38	18
2400	638	38	18	8
4800	318	18	8	3
9600	158	8	3	"-"
19200	78	3	0.5	"-"
38400	38	"-"	"-"	"-"

Table 1: Z8530SCC Divisional constants for different baud rates and divisional factors

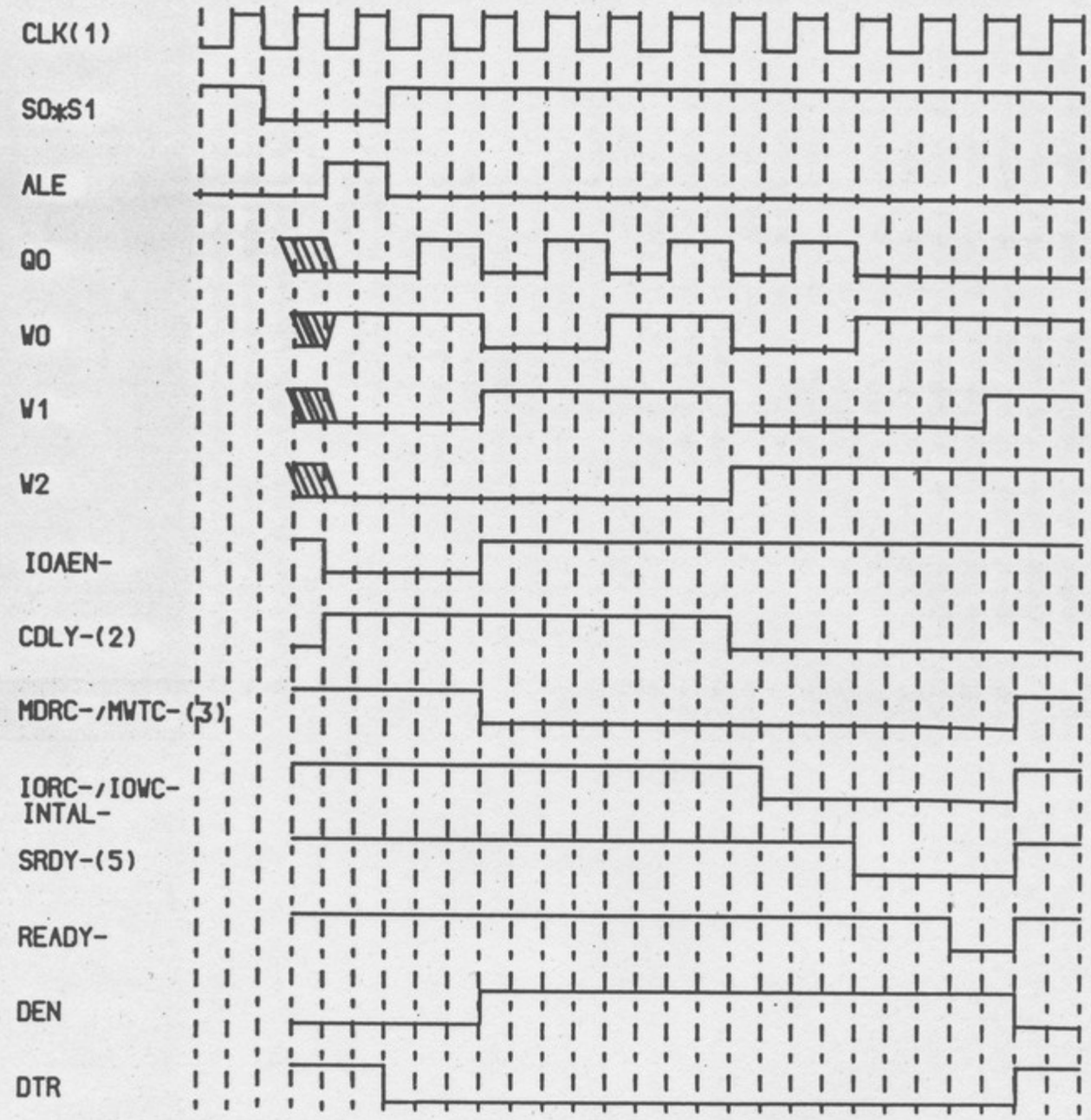


Figure 2 : Basic local bus cycle timing

Notes:
1. CLK cycle time is 62,5 ns or 83 ns.
2. Command delay starts only for the I/O cycles.
3. Local bus memory cycles have no command delay. It takes two wait states and satisfies 200 ns or 250 ns access time.
4. This waveform covers the SCC and PIC timing. RTC timing takes another wait state. NPX timing takes one wait state less.
5. This waveform covers the SCC and PIC timing.

4.1.2 REAL TIME CLOCK

There is an integrated circuit MC 146818 real time clock on the VME CPU/286 board, with a battery backup via the line +5V STB. The supply voltage is automatically switched from a standby mode into a normal one and vice versa. RTC maintains the time of the day, date and alarm time in its own internal registers accessible via the local bus. When the clock of the real time reaches the alarm time the interrupt request on level 1 of the interrupt controller 8259A is generated. RTC incorporates also a generator of a periodic signal (square wave) which generates the periodic interrupt request on level 0 of interrupt controller 8259A. The interrupt request on level 1 of the interrupt controller can be periodically generated.
The periods of the square wave signal and periodic interrupt can be program settable according to the table enclosed.
The RTC can not place interrupt vector (ID byte) on the local bus. For this reason 8259A ICW3 register bit 0 and bit 1 must be set to 0. That means 8259A interrupt controller will place interrupt vector on the local data bus.
The square wave signal is used for the generation of the system clock and interrupt request on level 1 of the interrupt controller for setting the alarm according to the real time.
RTC is driven by the oscillator with a frequency 4.194304 MHz. It incorporates also 50 additional RAM locations mapped on the IO address space and intended for general use.

rate select control register 1				periodic interrupt rate tpl	SQW output frequency
RS3	RS2	RS1	RS0		
0	0	0	0	none	none
0	0	0	0	30.517 us	32.768 kHz
0	0	1	0	61.035 us	16.384 kHz
0	0	1	1	122.070 us	8.192 kHz
0	1	0	0	244.141 us	4.096 kHz
0	1	0	1	488.281 us	2.048 kHz
0	1	1	0	976.562 us	1.024 kHz
0	1	1	1	1.953125 ms	512 Hz
1	0	0	0	3.90625 ms	256 Hz
1	0	0	1	7.8125 ms	128 Hz
1	0	1	0	15.625 ms	64 Hz
1	0	1	1	31.25 ms	32 Hz
1	1	0	0	62.5 ms	16 Hz
1	1	0	1	125 ms	8 Hz
1	1	1	1	250 ms	4 Hz
1	1	1	1	500 ms	2 Hz

Table 2: Periodic interrupt rate and square wave output frequency

4.2 DYNAMIC MEMORY

There is also dynamic memory of a capacity 128/256/512 Kb on the VME CPU/286 board. The memory capacity depends on the used integrated circuits DRAM (64 K bit, 128 K bit or 256 K bit), and it works in a dual ported mode which means the access is made possible from the part of processor 80286 or any other master on the VME bus. At the access to memory locations from the part of the VME bus, the central processor operates normally without HOLD states. The integrated circuit 8207 dual ported dynamic RAM controller takes care of the control of memory cycles, control of data buffers and solving of conflicts at the simultaneous access from the part of the central processor and the VME bus. An adequate jumper setting on a jumper field JRC helps to adopt the operation of this controller for:

- different capacities of used DRAM integrated circuits,
- different speeds of these circuits,
- different refresh periods of these circuits
- different speeds of the central processor (6MHz, 8MHz).

The central processor uses port A of controller 8207 when accessing memory in the synchronous mode. But when accessing memory from the part of the VME bus it uses port B in the asynchronous mode. At a simultaneous access to both ports, port A has a higher priority (central processor).

The memory cycle from the part of the central processor begins when a specially decoder circuit generates the select signal for the dynamic memory (RPEA-). The control over the time course of the cycle is taken over by circuit 8207, which takes care of an adequate generation of RAS, CAS, WRITE and A0-A8 signals, as well as signals for the control of data buffers, and signals for multiplexing of address lines of ports A and B. The cycle is completed when circuit 8207 generates MRDY- signal which tells the central processor the cycle is correctly completed. The memory cycle can take one or more wait states according to the settings of jumper field JRC.

In case of back-to-back cycles there is always at least one wait state if there are 64 Kb or 256 Kb memory circuits on the board. If there are DRAM integrated circuits 128 Kb on the board, an interleaving mechanism is activated, which enables the cycles without wait states, even in case where there are back-to-back memory cycles.

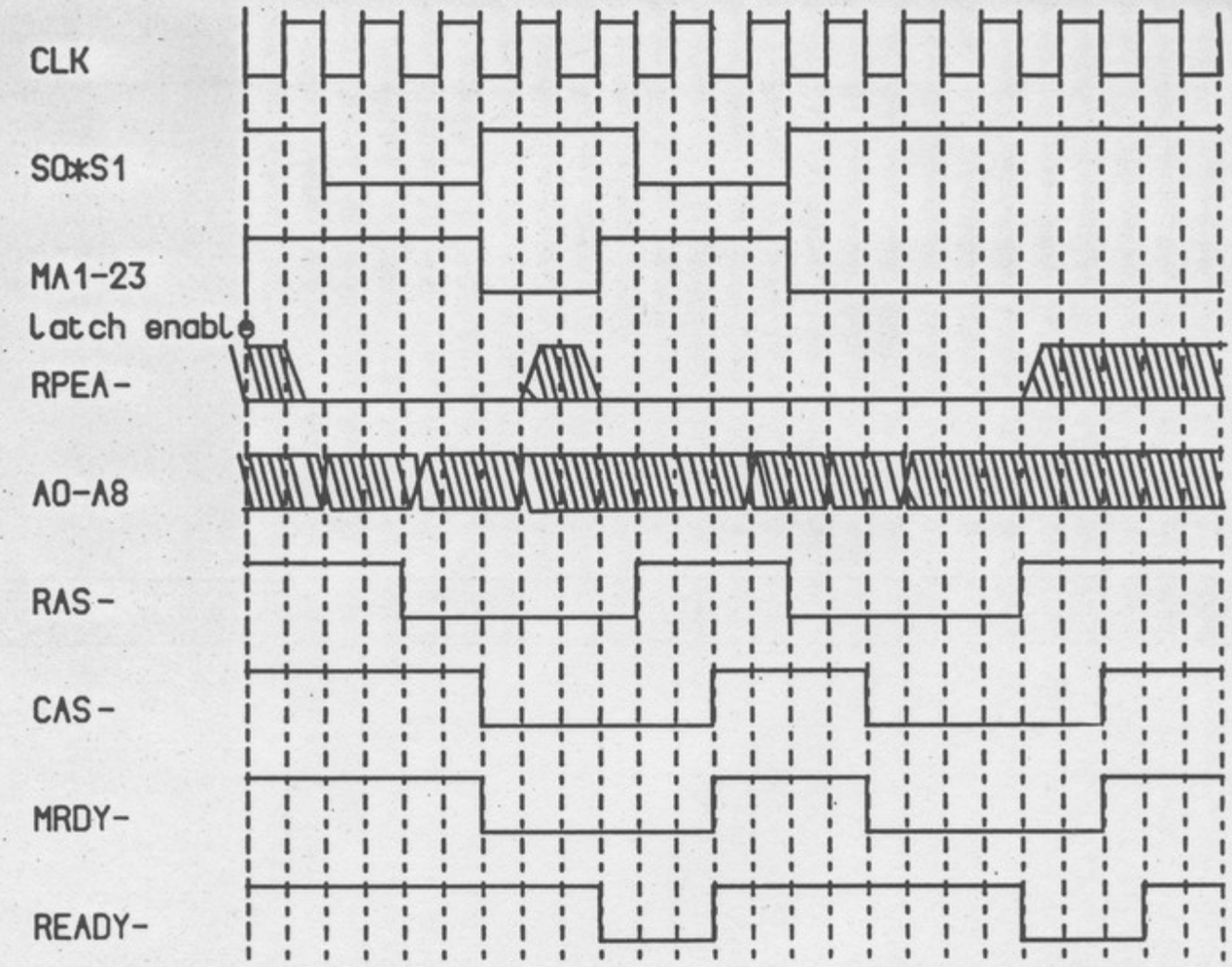


Figure 3 : Basic memory read cycle (zero wait state)
Notes:
- write cycle has a different timing waveform
- different JRC jumper installations can produce different timing waveform (more wait states)
- back-to-back cycle takes another wait state to satisfy DRAM RAS precharge time (second memory cycle shown).

The memory cycle from the part of the VME bus begins when a special address decoder circuit generates 8207 port B select signal RPEB- and simultaneously one of RD- or WR- commands is active. The RPEB signal is generated on the basis of the address lines of the VME bus A17-A23 when AS* (address strobe) is active. The RD- or WR- commands are generated on the basis of the VME bus WRITE* signal and VME bus data strobe DS0* or DS1* signals. The control over the time course of the memory cycle is taken over by circuit 8207 which takes care of appropriate generation of RAS, CAS, WRITE and A0-A8 signals as well as signals for the control of data buffers, signals for multiplexing of address lines of ports A and B. Circuit 8207 begins the final section of the cycle when it generates the XACKB- signal being transmitted on the VME bus as DTACK*. The VME bus master which began this memory cycle removes the AS*, DS0*, DS1 signals and the cycle is completed. The number of clock pulses from the beginning of the memory cycle (RPEB-, RD- or WR-) till the moment when XACKB- signal is generated, depends on different jumper settings on a jumper field JRC. The time from the moment when XACKB- is active till the actual end of the cycle depends on a time course of the events, being under control of the VME bus master which began this memory cycle.

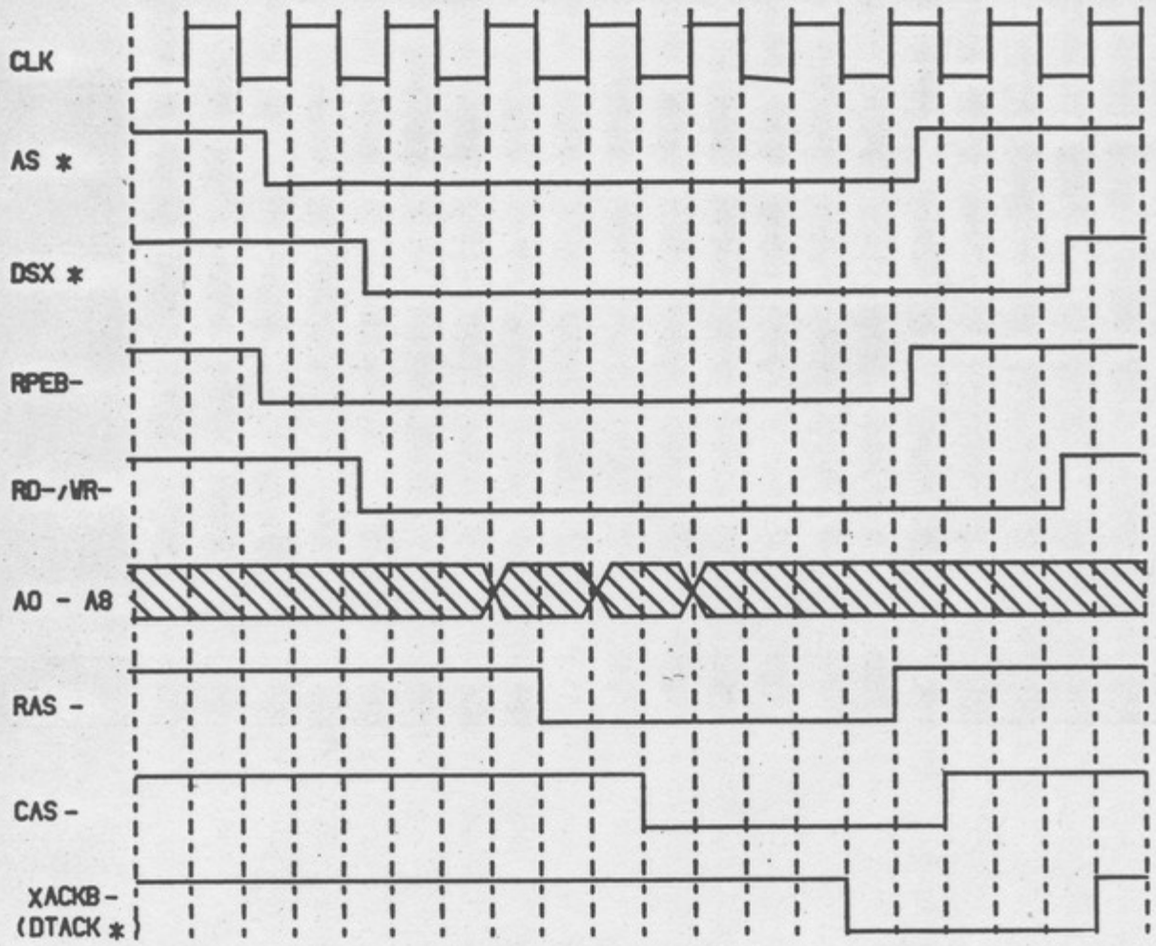


Figure 4 : VME CPU/286 Slave read timing

Notes:

- write cycle has different timing waveform
- different JRC jumper installations can produce different timing waveforms (more wait states)
- when generating the RPEB- signal 3D (hex) combination AM0-AM5 lines of the VME bus (standard supervisory access) are decoded.

4.3 VME BUS INTERFACE

When the central processor begins a bus cycle out of the address space of the local bus or dynamic local memory the LOCR signal is generated. This means the next cycle of the central processor will be a VME bus cycle. The cycle begins when the local bus requester is granted a permission to use VME DTB bus (active level of the AEN- signal). Then the drivers of address lines (A1-A23) are opened. At the same time the drivers of address modifiers (AM0-AM5), WRITE* and IACK* signals are opened. Simultaneously drivers of data lines D0-D15 are opened in the appropriate direction, depending on read or write operation. Two clocks later AS*, DS0*, and/or DS1* are set to active levels. The cycle is finished when one of the signals DTACK* or BERR* is activated. If none of this two signals activate in a predefined time, the cycle is completed automatically (bus time out), and the NMI interrupt is also generated on the central processor. VME DTB cycle is completed via ARDY- input of clock generator 82284, which finishes the cycle of the central processor on the VME bus.

4.3.1 VME DTB REQUESTER

LOCR signal, which means the request of a central processor for the data transfer through the VME DTB bus, latches first. Then it is transferred to the BR3* line of the arbiter bus. When the central processor occupies the VME DTB bus the signal is deactivated and remains deactivated until the central processor loses the control over the VME DTB bus. Before the request is deactivated the VME DTB requester activates the BBSY* signal, which means it occupied the VME DTB bus. The central processor can occupy the bus in case BBSY* and AS* are unactive and BG3IN* is active. The BG3IN* signal of the VME arbiter bus is set firmly in the active mode if the local VME bus arbiter is used. Otherwise this signal generates the system controller which takes care of the VME DTB bus arbiter.

The VME DTB requester removes the BBSY* signal when the central processor starts the bus cycle which accesses the local dynamic memory or the local bus (release when done). The VME DTB requester removes the BBSY* signal also if during the operation of the VME DTB data transfer The BR3* signal is activated (release on request).

4.3.2 VME BUS ARBITER

The VME CPU/286 can operate in the system without the system controller by using on-board option ONE VME bus arbiter. The task of this arbiter is to generate the BG3OUT* signal regarding the state of the following signals BR3*, BBSY* and LOCR, which represents the local request for the use of the VME DTB bus. The BG3OUT* signal is generated if the BBSY* and LOCR are not active and BR3* is active. In this case the BG3IN* signal must be fixed at the active level with the jumper on the jumper field JBG. The BG3OUT* signal is generated regardless the state of the AS* signal which means the arbiter functions during the last cycle which improves throughput of the DTB bus.

4.3.3 INTERRUPT HANDLER

The nucleus of the interrupt handler is an integrated circuit 8259A programmable interrupt controller (PIC). The PIC is connected to the local bus of the VME CPU/286 board, all its registers are accessible, which enable the choice of various modes of operation, priority setting of eight interrupt request inputs and masking of these inputs. The PIC generates the interrupt request signal for the central processor (INTR), if there is an active level on any of the eight interrupt request inputs of the PIC and if it is enabled.

The central processor reacts to the active level of the INTR

signal if the IF bit is set in the status and control register (interrupts enabled). The central processor reacts to the INTR in a way that starts two successive interrupt acknowledge cycles. In the time of the first cycle the 8259A circuit resolves priorities and detects the source of the ID byte regarding the operation mode of this circuit being chosen at the initialisation. The ID byte can generate the 8259A circuit itself for any of the eight interrupt request inputs or it is generated by the device which generated the interrupt request. The central processor reads the ID byte in the second interrupt acknowledge cycle.

The VME interrupt request lines IRQ1*-IRQ5* are connected to the interrupt request inputs of the 8259A circuit IR6-IR2 in the same succession.

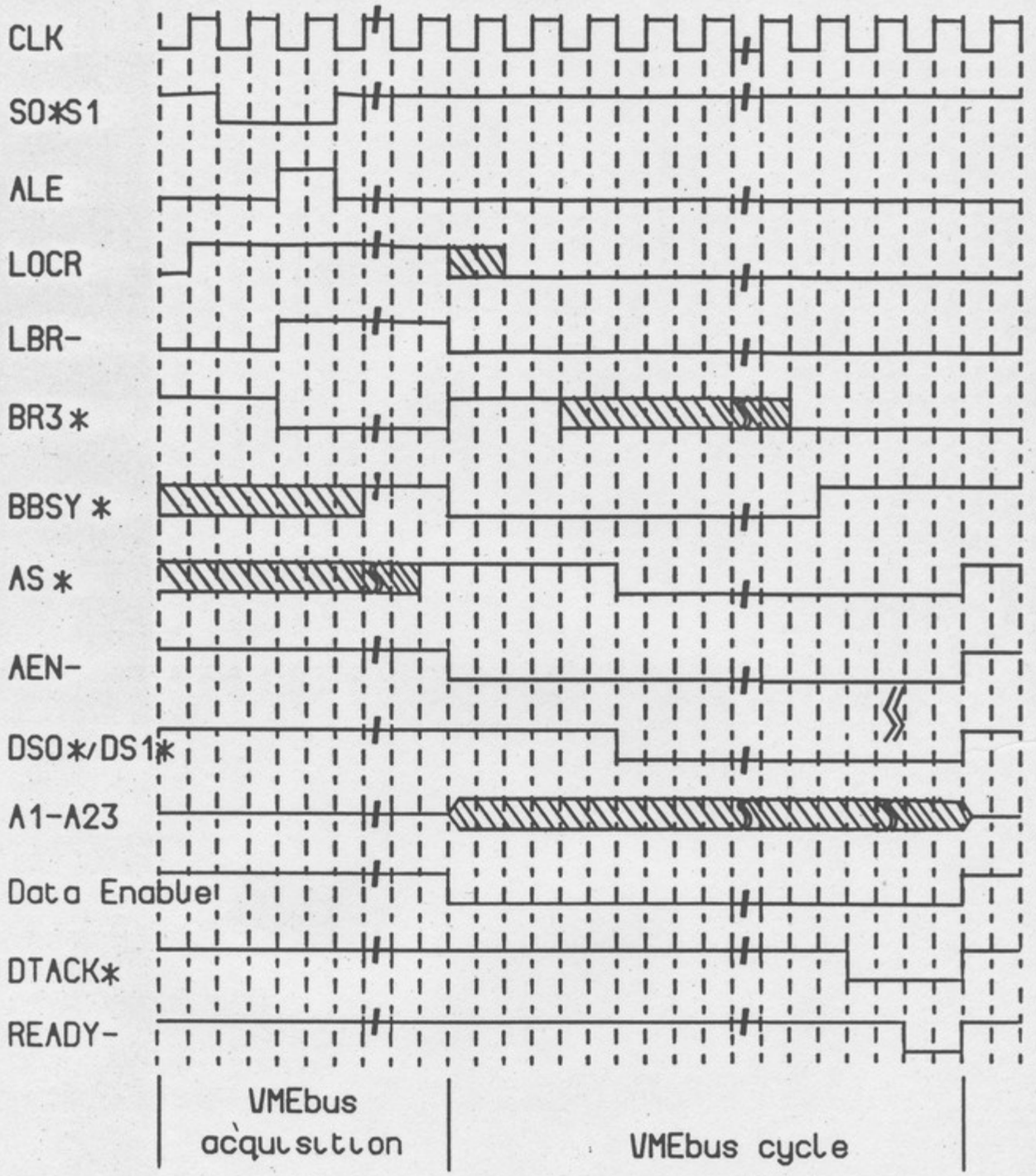


Figure 5 : Basic VME bus acquisition with the VME bus cycle

Notes:

- WRITE* has a stable level when AEN- goes down
- IACK* has a high level
- DTACK* goes up after DS0* or DS1* goes up
- while "data enable" is low, data buffers are open in the appropriate direction.

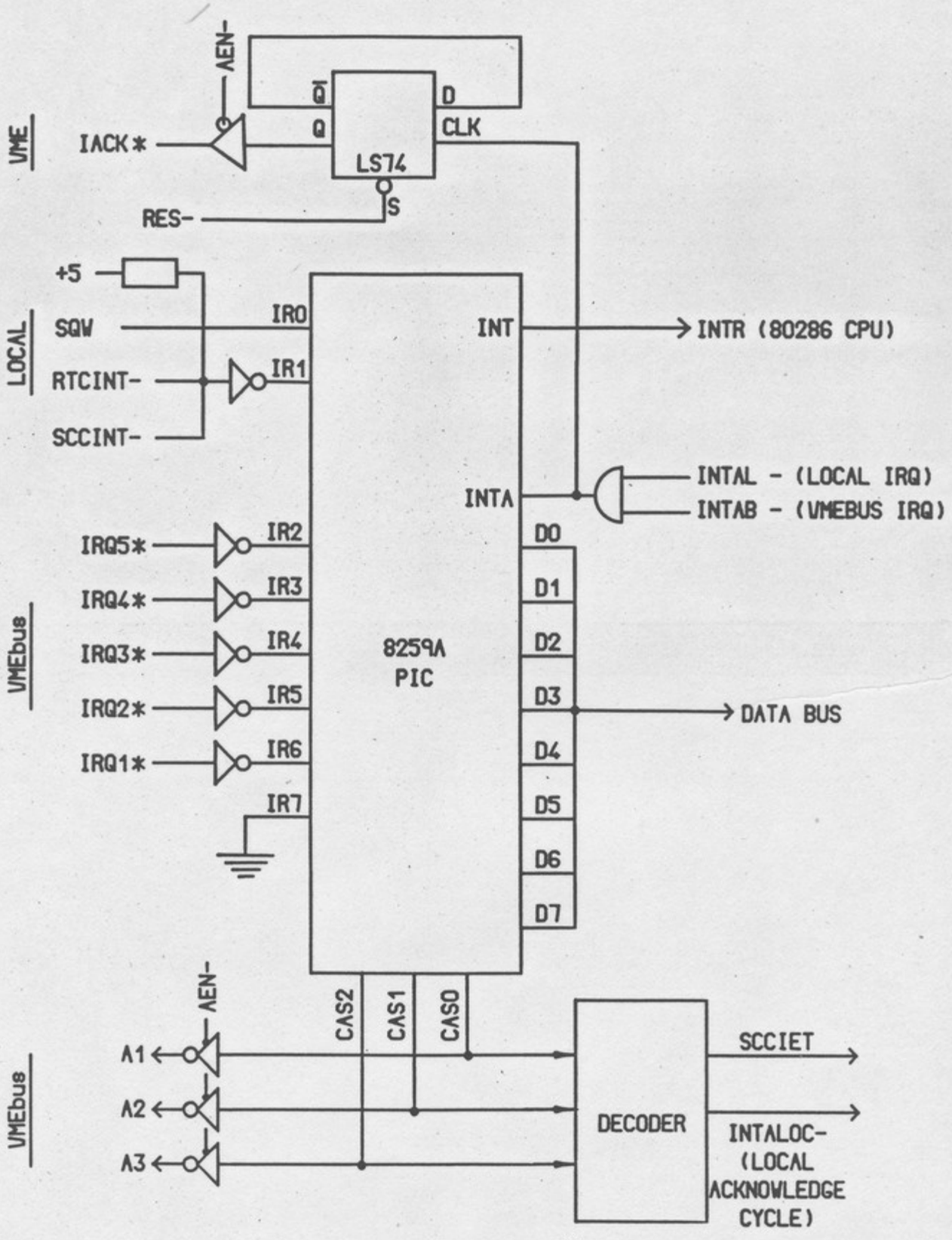


Figure 6 : Basic circuit for the processing of the local and VME bus interrupts IRQ1*-IRQ5* (interrupt handler)

Izdaja	1					List	Stran	J	K	Identifikacijska številka
Št. obvestila	11-017					24				33837044
Iskra Delta proizvodnja računalniških sistemov in inženiring, p.o.						Arhiv				Namesto identifikacijske številke: 22067044

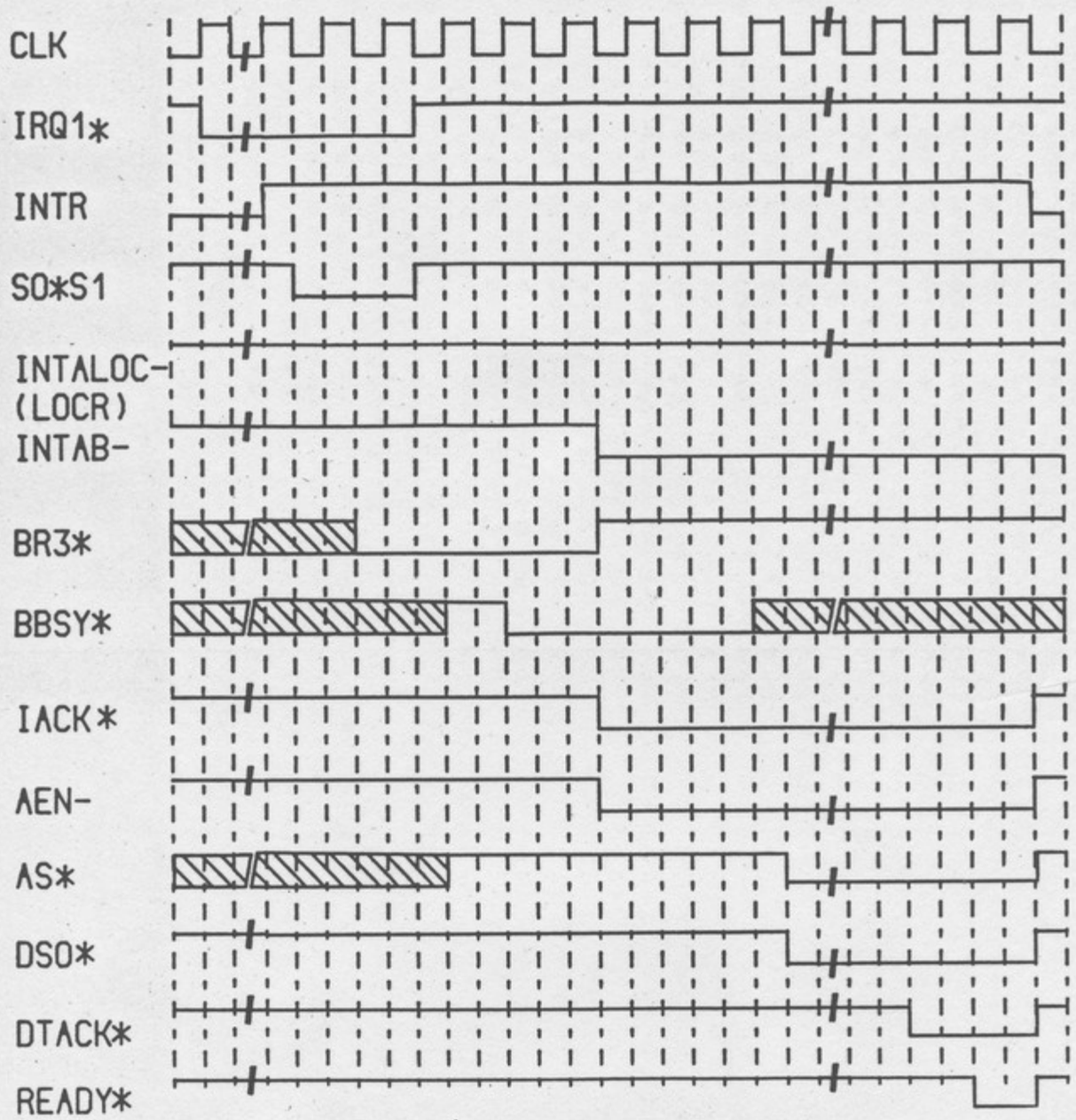


Figure 7 : Basic VMEbus interrupt acknowledga cycle

Notes : The first central processor interrupt acknowledge cycle accesses PIC on the local bus without any data transfer.
- Non active INTALOC- level is set during the first interrupt acknowledge cycle.
- AEN- active level means that it is allowed to begin the VMEbus cycle.

The local interrupt request SQW and SCC viz. RTC are connected to IR0 and IR1 inputs of the PIC. The circuit differs the local interrupt acknowledge cycles from the VME bus ones on the basis of the INTALOC- signal, which is active when the local (on-board) interrupt requets are serviced. The INTALOC- signal is generated on the basis of the following signals CAS0, CAS1 and CAS2 being generated by the PIC in the cascade mode (ICW1 register, SNGL bit=0). These three signals give the binary code of the interrupt request input having at the moment the highest priority and its ID byte (vector) is placed on the local data bus in the running interrupt acknowledge cycle. The PIC generates the ID byte for all interrupt request inputs which have an appropriate bit in the ICW3 register set to 0. If the bit is set to 1, then the ID byte is generated by the device which requested an interrupt. Therefore the ICW3 bits 2, 3, 4, 5 and 6 must be set to 0 for the VME bus acknowledge cycles. During the interrupt acknowledge cycles for the VME bus interrupt requests IRQ1* to IRQ5* the INTALOC- signal will remain inactive which represents a signal for the bus requester to begin the interrupt acknowledge cycle on the VME bus. The ICW3 bit 0 must always be set to 0 , since the real time clock circuit cannot generate the ID byte and for this reason PIC will always do it . If the bits 2, 3, 4, 5 and 6 of the ICW3 register of the PIC are set to 0, the PIC itself will generate the ID bytes for the VME bus interrupt requests IRQ1* to IRQ5*.

The interrupt acknowledge cycle on the VME bus begins when the INTALOC- signal is inactive during the second interrupt acknowledge cycle of the central processor. Then the VME bus requester demands the access to the VME bus so that it activates the BR3* signal. When the VME bus arbiter allows the use of the bus (AEN- active) the interrupt acknowledge cycle begins with the active signal IACK* and address lines A1, A2 and A3 which identify the VME bus interrupt request level which is serviced at the moment.

5. PROGRAMMING MODEL

This chapter is intended to help programers write programs for this board. Here are included only programming considerations related on VME CPU/286 board architecture and HW solutions. Especially here are few words about managing IO devices attashed on the VME bus. All Programming informations you can find in VME CPU/286 Software guide and iAPX 286 Programmers Manual.

5.1 Memory and IO map

The VME CPU/286 board is based on the processor 80286 which differs the memory and the IO address space. The memory address space of this processor has a capacity of 1Mb in the real address mode viz. 16 Mb in the protected and virtual address mode (PVAM). On the board itself there are memory elements occupying part of the address space. The dynamic memory of a capacity 128 Kb, 256 Kb or 512 Kb has its beginning in the physical address 0. A maximum capacity of EPROM memory comprises 64KB and occupies the final section of the memory address space. The starting address of EPROM in the real address mode is on the physical address F0000. In the PVAM mode the starting address of EPROM is in the physical address FF0000. A transfer from the real address mode to the PVAM mode is made by setting an appropriate bit in the control register of the central processor and by the write to any EPROM location. If EPROM with lower capacities than 32K byte are put in the EPROM sockets the starting address moves accordingly upwards. In each case the memory space F0000 through FFFFF or FF0000 through FFFFFF is occupied and EPROM repeat in this address space.

EPROM	starting address	repetition
2732	(F) FE000	8 x
2764	(F) FC000	4 x
27128	(F) F8000	2 x
27256	(F) F0000	-

Starting addresses and repetitions for different EPROM's

The IO address space of 80286 processor is 64 Kb. On the VME CPU/286 board the addresses 0 through FF(hex) are occupied for accessing the registers of local IO devices (SCC, RTC, PIC and NPX). The registers of local IO devices are eight bit and data are transferred through data lines D0-D7 for all IO devices but the numerical coprocessor (NPX).

device	address	repetition
RTC	0-7F	-
SCC	80-BF	8 x
PIC	C0-DF	8 x
NPX	E0-FF	note 1

Note 1: Intel has reserved addresses FC-FF(hex) of the IO address space for the communication of the central processor with the numerical coprocessor 80287. The decoder of the addresses of the IO devices and the numerical coprocessor does not decode all of the address lines A1 through A15. For this reason repetitions of the registers occur on the local IO address space. The communication between the central processor and the NPX coprocessor is made by using all 16 data lines.
Data bits D8 through D15 of the local bus during IO read operations transfer the state of the status register which contains the information on the source of the NMI interrupt and the state of the VME bus SYSFAIL* signal.

The state of the status register can be read by read port command in any even address in the 0 through DF(hex) IO address space segment.

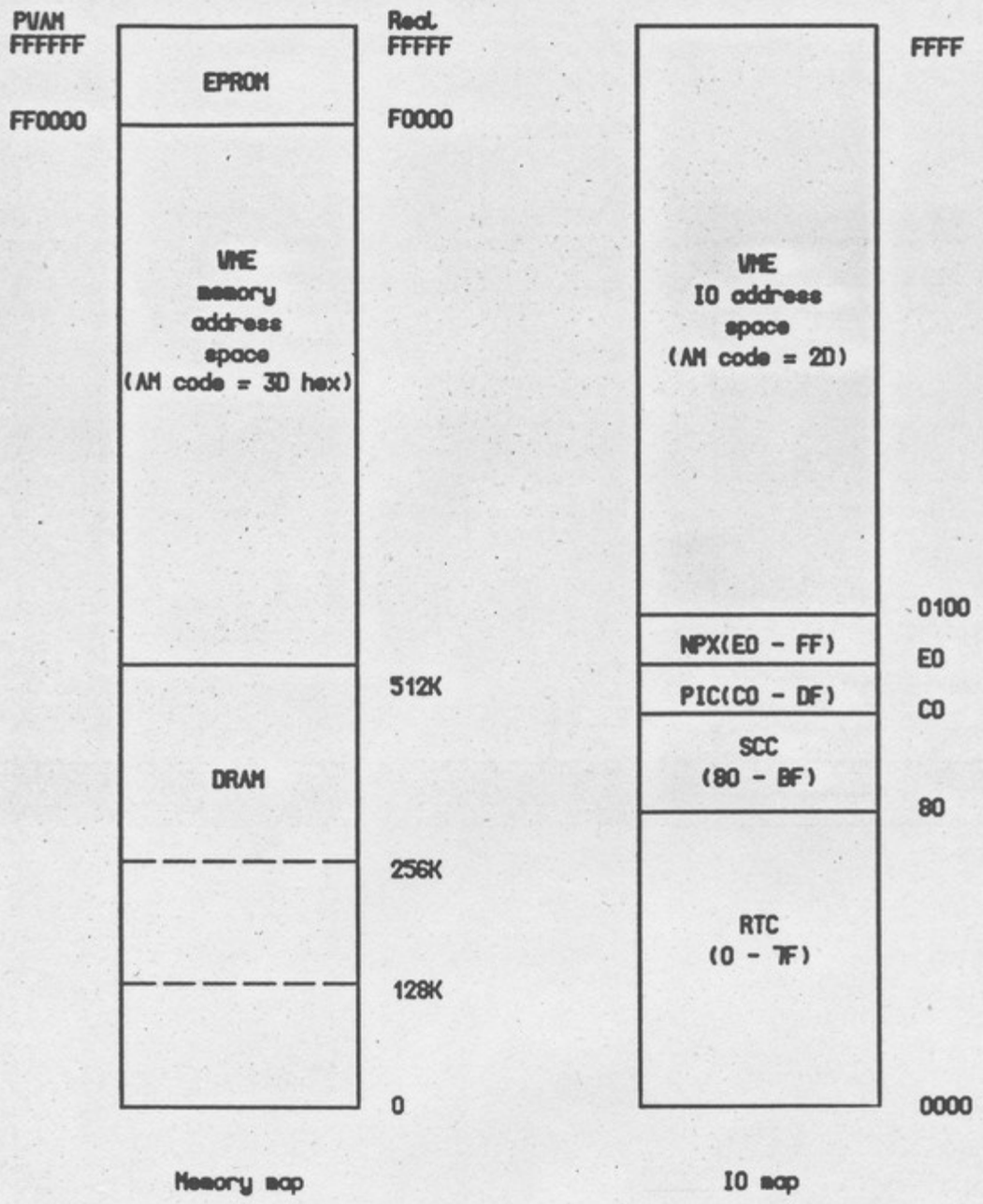


Figure 8 : Memory and IO map

Izdaja	1				
Št. obvestila	11-017				

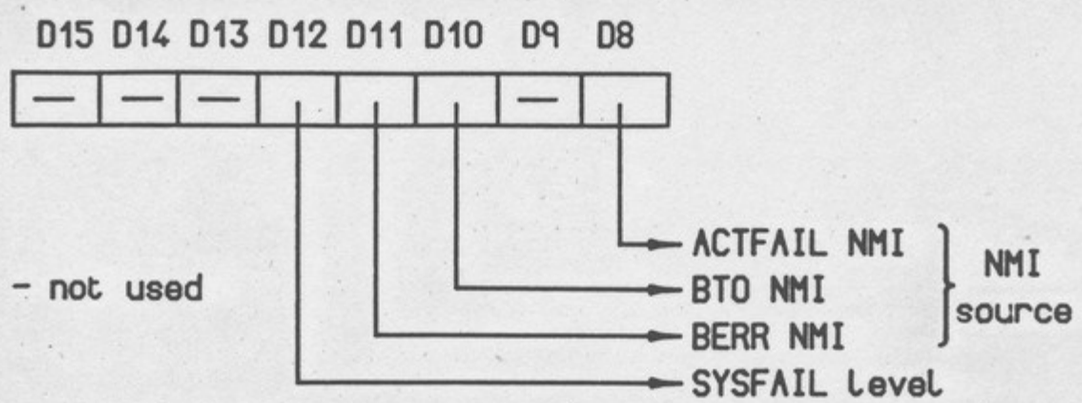
List	Stran	J	K	Identifikacijska številka
29				33837044

Arhiv

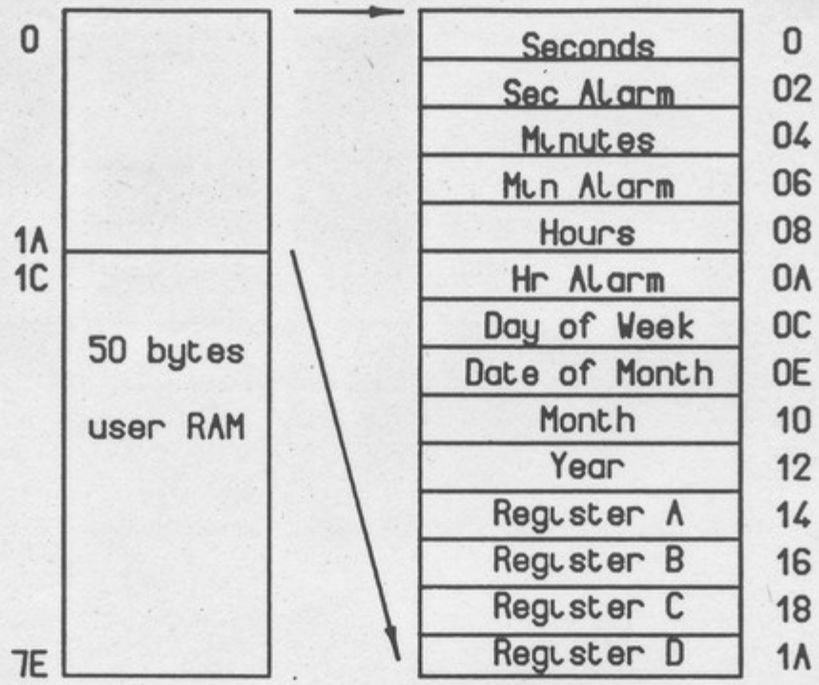
Namesto identifikacijske številke: 22067044

IskraDelta
proizvodnja računalniških sistemov in inženiring, p.o.

saro 82-3407-12-84



VME CPU-286 Status register



RTC Register Map

80	Control B
82	Data B
84	Control A
86	Data A

SCC Register Map

C0	A0 = 0
C2	A0 = 1

PIC Register Map

Figure 9 : VME CPU/286 Input/Output Register Map

5.2. iAPX 286 - VME bus programming consideration

When programming diferent IO devices attashed on the VME DTB bus keep in mind that iAPX 286 processor transfers even bytes by VME bus data lines D0 - D7 and add bytes by VME bus data lines D8 - D15. Usually it affects original register addresses asignment specified in the users manual at such devices. In general odd addressed registers become even and vice versa. For example here we have original and affected address asignments for WFC-1 (Force Computers Advanced Systems) Winchester and Floppy drive controller with base address 8000 (hex):

original	affected	Read Register	Write Register
8000	8001		CI Vector Register
8001	8000	Data Register	Data Register
8002	8003		Data Req Vector Reg
8003	8002	Error Register	Write Precomp
8005	8004	Sector Count	Sector Count
8007	8006	Sector Number	Sector Number
8009	8008	Cylinder Low	Cylinder Low
800B	800A	Cylinder High	Cylinder High
800D	800C	Size/Drive/Head	Size/Drive/Head
800F	800E	Status Register	Command Register

Note that all local (on board) and VME bus memory address space behaves the same way. For example next instructions produce memory image as shown:

```
                                        MEMORY

    MOV  AX,S55AA
    MOV  BX,LOW                  LOW+1 55
    MOV  BX , AX                 LOW   AA
```

Some problems may arise in multiprocessor configurations if we have mixed masters with diferent even/odd byte assignment.

In systems with DMA data transfers memory to serial device and vice versa the serial bit stream will have different bit sequence (low byte, high byte) than in systems with processors with VME bus compatible even/odd byte assignment.
All this even/odd assignment problems may be selved at SW level.

Note that VME CPU/286 operates in two diferent modes: Real and PVAM. In real mode processor can address up to 1Mbyte memory space while in PVAM mode this space is 16Mbyte. If you want to utilize all 16Mbytes VMEbus address space., and to run processor in protected mode you have to switch processor and on board logic to PVAM mode by next software sequence:

```
    mov bx,0              ;switch local logic
    mov $eooo:$bxC,al
    smsw ax               ;switch 80286
```

```
or ax,1
lmsw ax
```

Before switching procesor and logic to PVAM mode you have to initialize GDT and IDT CPU registers as a pointers to Global Descriptor Table and Interrupt Descriptor Table.

5.3. VME bus interrupt processing

Before starting to process on board and VME bus interrupt requests 8259A Programable Interrupt controller must be initialized. There are many interrupt processing modes and configurations which can be set up with different 8259A initialization sequences (see 8259A data sheat). For each interrupt request level (7 levels) we can specify source of ID byte and activity (enabled/disabled). Also we can choose beetwen diferent priority shemes, nesting and diferent and-of-interrupt sequences.

For VME bus IRQ1 - IRQ5 processing we have possibility to choose ID byte source. If ID byte source is interrupter than apropriate bit in 8259A ICW3 register must be set to 1. If ID byte source is not interrupter than appropriate bit in 8259A ICW3 register must be set to 0. VME bus interrupt request processing with on board (VME CPU/286) ID byte source is possible only with interrupters with possibility to remove interrupt request under software control (read status, write command ...). Note that all VME bus interrupters have no such possibility.

Next example will show Programable Interrupt controller initialization sequence for edge triggered requests base interrupt ID byte 40 (hex), IRQ1 - IRQ5 requester ID byte source, periodic and SCC interrupt requests Programable Interrupt controller ID byte source and automatic End of Interrupt mode, all interrupt requests enabled:

```
MOV  AL,S15 ; edge triggered, cascade mode
OUT  SC0,AL
MOV  AL,S40 ; base ID byte
OUT  SC2,AL
MOV  AL,SFC ; IRQ1 - IRQ5 Requester ID byte source
OUT  SC2,AL
MOV  AL,S0F ; Auto EOI, buffered mode,
OUT  SC2,AL
MOV  AL,0
OUT  SC2,AL ; all IRQ's enabled
```

In the multiprocessor system configurations (more VME CPU/286 in one system) there are need for locked bus operations (Read-Modify-Write DTB cycles). Purpose of this type of cycles is to protect sequence of DTB operations being interrupted. Some 80286 CPU instructions implicitly start Read-Modify-Write cycle. Such instruction is Exchange byte or word instruction (XCHG). Note

that 80286 CPU has possibility to append LOCK prefix to any instruction. To start Read-Modify-Write cycle use only such instructions which make two consecutive references to the same location (like XCHG).
Read-Modify-Write cycles are possible only when accessing operands in global (non local) memory.

6. INSTALATION

6.1. Jumper settings

There are several jumper places on the VME CPU/286 board for the choice of different modes of operation of separate functional modules. The following choices are possible:

BR1 the choice of speed of the central processor (6MHz or 8MHz)

JNPX the choice of speed of the numerical coprocessor (5MHz or 8MHz)

JEPR the choice of capacity of the installed EPROM's (24 pin or 28 pin)

JJ2, JJ3 configuration of RS232 channels and signal strapping Modem control signals may be conected to +12V to be active all the time or conected to the comunication device throu conectors J2 or J3.

JMP switch on/off on-board SYSCLK* generator

JBG BG3IN* strapping (VMEbus arbiter option)

JRC DRAM configuration regarding the capacities and speeds of DRAM circuits and the speed of the processor

JIACK IACKIN*/IACKOUT* chain start option

BR1: The choice of speed of the central processor is necessary since two speeds (either 6MHz or 8MHz) of the central processor can be used. If pins 1 and 2 of the jumper field BR1 are connected, the internal oscillator of the clock generator 82284 oscillates on crystal 12 MHz, which is suitable for the processor 6MHz. If pins 1 and 2 are not connected the clock generator uses input EFI as a source of a basic frequency got from the VME bus SYSCLK* or 16 MHz on-board oscillator Q4, depending on jumper settings on jumper field JMP: BR1 is left unconnected if an 8 MHz processor is used.

JMP: It enables the use of the on-board 16 MHz oscillator for the generation of the SYSCLK* VME bus clock, the use of SYSCLK* clock for the drive of the local processor and the use of the on-board 16 MHz oscillator for driving the local processor.

jumpers	function
1-2	the processor operates with 8 MHz (BR1 open)
3-4	the on-board 16 MHz oscillator drives SYSCLK*
2-4	the processor operates with 8 MHz (BR1 open) on the basis of the SYSCLK* clock

If the board does not operate in the system as the bus arbiter, then pins 2 and 4 of jumper field JMP should be connected and pins 1 and 2 of jumper field BR1 unconnected.
JNPX: It determines the speed of the operation of the numerical coprocessor. The use of 5 MHz or 8MHz numerical coprocessor is possible.

coprocessor used	JNPX settings
80287-3(5 MHz)	2-5, 3-4
80287 (8 MHz)	1-6

JEPR: It enables the use of EPROM circuits of different capacities. Settings for 24 pin EPROM's and 28 pin EPROM's are to be distinguished.

EPROM	settings
24 pin	3-4
28 pin	1-2

JBG: When the board operates as the VME bus arbiter then pins 1 and 2 should be connected. If the module operates in the system with a special VME bus system controller then pins 1 and 2 are left disconnected. In this case the processor should use SYSCLK* as the source of the basis clock (BR1 open, JMP:2-4 conected).

IACK: If the module is installed in slot 1 of the VME bus rack (VMEbus arbiter), then pins 1 and 2 should be connected, otherwise not. When connecting pins 1 and 2, the signal IACK* is connected with the chain IACKIN*/IACKOUT* of the VME bus.

JRC: It enables the adaptation of different speeds and capacities of DRAM circuits and different speeds of the central processor.

capacity	installation
128 Kb (64 Kbit IC's)	7-10, 8-9
256 Kb (128 Kbit IC's)	8-9
512 Kb (256 Kbit IC's)	7-10

processor 80286	installation
6 MHz	-
8 MHz	5-12

DRAM trac	installation
< 150 ns	6-11
150 ns	-
200 ns	cannot be used

DRAM refresh period	installation

128/2 ms or 256/4 ms	3-14
256/2 ms	-

refresh period correction	installation
0 %	1-16, 2-15
10 %	2-15
20 %	1-16
30 %	-

extended cycle	installation
yes	4-13

JJ2, JJ3: They enable the configuration of RS2232 channels as data terminal equipment (DTE) and strapping of modem control signals.
Pin 16 of jumper field JJ2 or JJ3 is used for a possible strapping of modem control signals (RTS; CTS, DSR, DCD, DTR). At the installed male connector D25 (DTE) modem control signals are connected by jumpers 8-13, 7-14, 10 - 11, 6-15, 9-12, and the receiver clock and transmitter clock 2-19 and 3-18 on jumper fields JJ2 and JJ3. All input modem control signals (CTS, DSR, DCD) are conected to +12V at factory.

6.2. System configuration considerations

From the systems configuration point of view we have to care about right on board jumper settings and VME bus backplane daisy chains connections.

When assembling VME bus based system with VME CPU/286 board we have two different situations: VME CPU/286 is used as a VME bus DTB Arbiter (Option ONE) or VME CPU/286 is used in system with special VME bus DTB Arbiter (Option ONE or PRI, Note that VME CPU/286 can not be used in systems with option ROR DTB Arbiters).

When assembling systems with VME CPU/286 board as a VME bus DTB Arbiter jumpers JBG and JIACK on the printed circuit board must be connected. Also, pins 1-2 and 3-4 of the jumper field JMP must be connected. In this case VME CPU/286 board must be located in slot 1 of the VME bus backplane. Pins B10 and B11 of the connector in slot 1 of the backplane must not be connected. All DTB requesters (located in any backplane slot but slot 1) must have connected BG3IN/BG3OUT daisy chain through logic of the requesters located closely to slot 1 or through BG3IN/BG3OUT jumpers in free slot positions or slot positions with passive boards (no requester). The same is with interrupt acknowledge daisy chain (IACKIN*/IACKOUT*). All boards with interrupt requesters must have connected IACKIN*/IACKOUT* daisy chain to the slot 1 through logic of the interrupt requesters, located

closely to slot 1 or through BG3IN*/BG3OUT* jumpers (backplane) in free slot positions or slot positions with no interrupter boards.
When using VME CPU/286 in system with special DTB Arbiter (Another VME CPU/286 in slsot 1 or any other board in slot 1 with DTB Arbiter Option ONE or PRI) jumpers JBG and JIACK must be open. Pins 2 and 4 of jumper field JMP must be connected and pins 1 and 2 of jumper field BR1 must be open. VME CPU/286 will connect chains BG3IN*/BG3OUT* and IACKIN*/IACKOUT* through its on board logic.

6.3. Installation notes

After preparing all the system components (backplane jumper setings and power supply connections, on boards jumper installations ...) put the boards into the VME bus rack. Note that from this moment it is important into which slot to install particular board because of decided Arbitration sheme and DTB requests priority or interrupt requests priority.

Do not put in or out any board from the VME bus rack while power is switched on. Be shure all DC power lines at backplane (+5VDC, +12VDC, -12VDC) are not out of range.

After power on switch proceed by using VME CPU/286 SW User's manual.

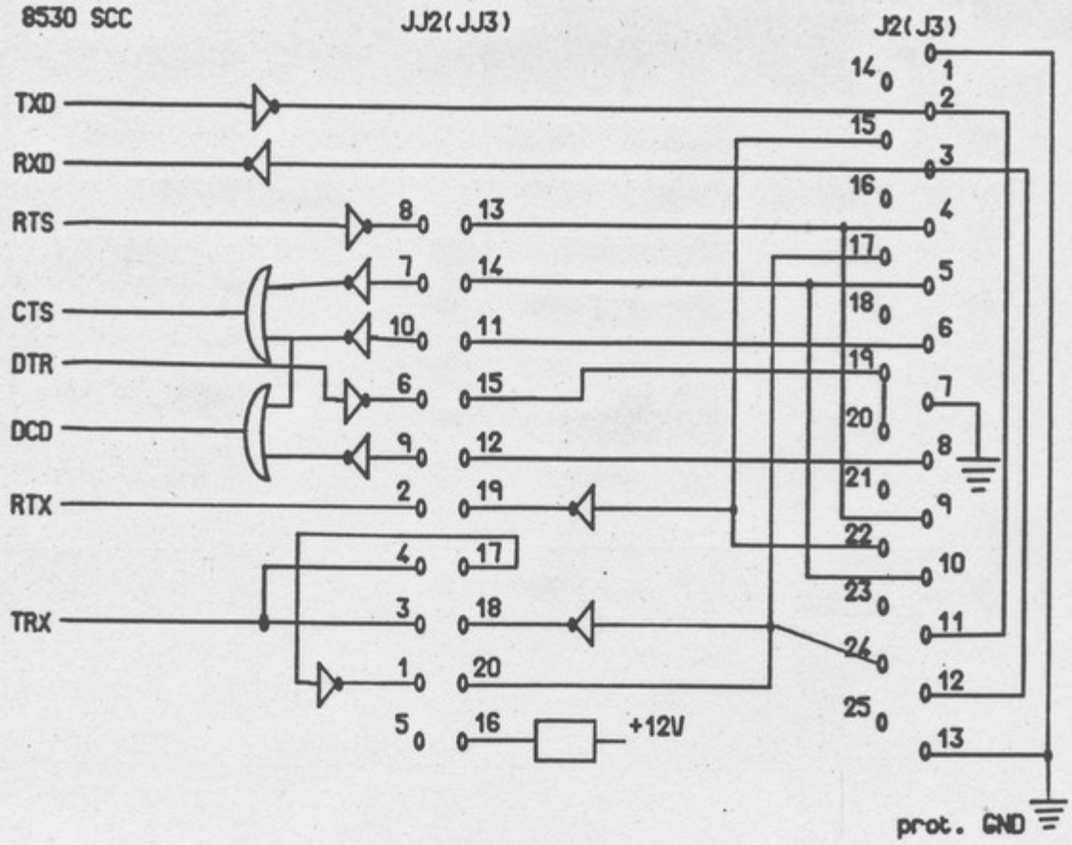


Figure 10 : JJ2 and JJ3 jumper field conections

Izdaja	1					List	Stran	J	K	Identifikacijska številka
Št. obvestila	11-017					38				33837044
IskraDelta proizvodnja računalniških sistemov in inženiring, p.o.						Arhiv		Namesto identifikacijske številke		2206704 4

Obr. 38

7. FRONT PANEL

On the front panel of the board there are two RS232 connectors and three LED's showing the status of the processor. The red diode means the processor is in HALT state. The yellow diode means the interrupt is waiting for service and the green diode means the normal operation of the processor.

These three diodes enble also simple diagnostics of the board in case of troubles. At least one of RUN or HALT (red, green) lights should always be on.

The reset key of the front panel is directly connected with the SYSRESET* VME bus signal and connects it to GND when pressed. In this way all modules on the bus can be reset, including the VME CPU/286 board.

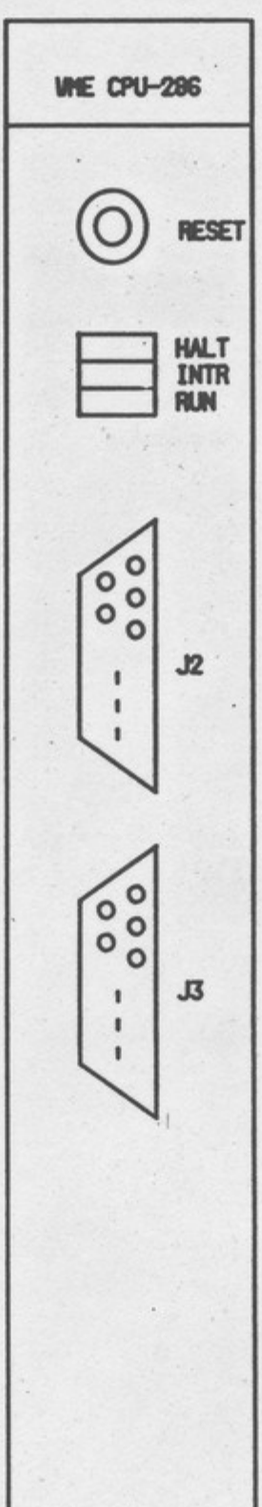


Figure 11 : Front panel

8. SPECIFICATION

GENERAL

description	Intel 80286/287 VME single board computer
configuration	DTB master, Option A24.D16 DTB slave, Option A24.D16
VME bus arbiter	Option ONE, single level
Interrupt handler	five IRQ lines: IRQ1-IRQ5
VME bus requester	BR3 Option ROR, RWD
power	+5VDC, 3 Amps (typ) +12VDC 0,40 Amps (RS232 only) -12VDC 0,60 Amps (RS232 only)
size	160 x 234 mm (double)
construction	6 layer printed circuit
temperature	0-70 degrees C operating
humidity	90 % non condensing (max)

MICROPROCESSOR

device	80286/287
clock frequency	8 MHz
data width	16 bits
addresssing	24 bits with memory management

SERIAL I/O

device	One Z8530SCC
number	two parts
type	synchronous or asynchronous
speed	programmable 300 - 1M baud
signal compatibility	RS232-C

MEMORY

array	sixteen, 16 pin sockets for DRAM two 28 pin sockets for EPROM
capability	128 KB - 64 K IC'S 256 KB - 128 K pigy IC'S 512 KB - 256 K IC'S

REAL TIME CLOCK

device	MC146818
technology	CMOS
capability	seconds, minutes, hours, days periodic interrupt, alarm

9. VME BUS CONECTOR J1/P1 PIN ASSIGNMENT

pin	row A	row B	row C
1	D00	BBSY*	D08
2	D01	BCLR*	D09
3	D02	ACFAIL*	D10
4	D03	BG0IN*	D11
5	D04	BG0OUT*	D12
6	D05	BG1IN*	D13
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GND
10	SYSCLK	BG3IN*	SYSFAIL*
11	GND	BG3OUT*	BERR*
12	DS1*	BR0*	SYSRESET*
13	DS0*	BR1*	LWORD*
14	WRITE*	BR2*	AM5
15	GND	BR3*	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	SERCLK	A17
22	IACKOUT*	SERDAT	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	-12V	+5V STDBY	+12V
32	+5V	+5V	+5V

10. RS232C DTE AND DCE CONECTOR PIN ASIGNMENT

pin	name	to DTE	to DCE	function
1	FG			protective ground
2	TD		->	transmitted data
3	RD	<-		received data
4	RTS		->	request to send
5	CTS	<-		clear to send
6	DSR	<-		data set ready
7	SG			signal ground
8	DCD	<-		data carrier detect
9	-			
10	-			
11	-			
12	-			
13	-			
14	-			
15	TC	<-		transmitter clock
16	-			
17	RC	<-		receiver clock
18	-			
19	-			
20	DTR		->	data terminal ready
21	-			
22	-			
23	-			
24	(TC)		->	external transmitter clock
25	-			

Device behaves as DTE (Data Terminal Equipment) regardless which conector is installed on the board (male or female).

11. WORST CASE ANALYSYS

Worst case analysis for next VME CPU/286 cycles has been done:

1. EPROM cycle
2. SCC cycle
3. PIC cycle
4. RTC cycle
5. NPX cycle
6. DRAM cycle
7. VMEbus master cycle
8. VMEbus slave cycle

1. EPROM cycle worst case (2732A, 2764A)

Reference EPROM cycle timming chart to identify times 1 and 2.

1 3 tCLK - t13 (CPU) - td (IC6) - td (IC15) =
187,5 - 60 (max) - 25 (max) - 10 (max) = 92,5 (min)
92,5 > 20 ns (t8 - 82288-8 MAX)

2 CPU 80286-8 address hold time ensures time 2 higher than t9 min (82288-8) > 0

1 and 2 needed for 82288-8 to start any local bus memory or I/O cycle. (1 and 2 are the same for all memory or I/O local bus cycles).

tACC:

5tCLK - t16(82288-8) - tD(IC24,IC23) - tD(IC21,IC22) -
- t8(80286-8) =
= 312,5 - 15(MAX) - 15(MAX) - 15(MAX) - 10(min) =
= 257,5 ns(MIN) > 250 ns (tACCmax, 2732A,2764A)

tOE delay: tCLK - t16 (82288-8)-tD-(IC24/23)+t29(82288-8) =
= 625 - 0 (min) - 0 (min) + 20 (max) =
= 82,5 ns (max) < tACC - tOE = 200 - 70 = 130 ns
that means MRDC - (OE) does not affect tACC.

t9 (80286-8) min 5 ns ensures 82288-8 with its DEN and MRDC timing.

2. SCC cycle worst case

All times tX are related to Zilog 8530A SCC timming data.

Read & Write

t7, t9:
tCLK + t16(82288-8)MIN + tD(IC23/24)MIN-t30(82288-8)MAX=
= 62,5 + 3 + 0 - 20 = 45,5 > 0

t8: 7tCLK - t16(82288-8)MAX - tD(IC23/24)MAX + t30(82288-8)MIN=
= 437,5 - 15 - 20 + 3 = 405,5 > 80 ns

t11,t13: 10tCLK - tPCLK - t30(82288-8)MAX + t30(82288-8)MIN =
= 625 - 325,5 - 2- + 3 = 282,5 > 160
(PCLK = 3.072 MHz)

t12,t14: 8 tCLK + t30(82288-8)MAX + t30(82288-8)MIN =
= 500 + 20 - 3 = 517 > 0

t16,t19: 7tCLK - t16(82288-8)MAX - tD(IC5)MAX + t30(82288-8)MIN =
= 437,5 - 15 - 25 + 3 = 400,5 > 0

t17,t20: tCLK + t16(82288-8)MIN +tD(IC5)MIN - t30(82288-8)MAX =
= 62,5 + 3 + 0 - 20 = 45,5 > 0

t18,t21: 7tCLK - t16(82288-8)MAX - tD(IC5)MAX + t30(82288-8)MIN=
= 437,5 - 15 - 25 + 3 = 400,5 > 70

t22,t28: 4tCLK = 250

read data access: 4tCLK - t29(82288-8)MAX - t25(SCC)MAX -
- t8(82286-8)MIN - tD(IC21/22) =
= 250 - 20 - 180 - 10 - 20 = 20 > 0

write data setup time - t29:
4tCLK - tD(IC30)MAX - t26(82288-8)MAX -
- tD(IC21/22)MAX + t30(82288-8)MIN =
= 250 - 10 - 25 - 20 + 3 = 208 > 0

Interrupt acknowledge:

t38: more than enough because INTA - is generated during first 80286-8 interrupt acknowledge cycle and it is valid for the second one.

t41: IEI allways active

data access: same as for read cycle

3. PIC cycle worst case (8259A-2)

All times tXXX are related to Intel 8259A-2 timming data.

Read, Interrupt acknowledge cycle:

tRLRH (read/inta):
4tCLK - t29(82288-8)MAX + t30(82288-8)MIN =
= 250 - 20 + 5 = 235 (MIN) = tRLRH(MIN)

tAHRL (cs-/AO to read/inta):
7tCLK - t16(82288-8)MAX - tD(IC23/24)MAX + t29(82288-8)MIN=
= 375 - 15 - 20 + 3 = 343 > 0 (tAHRL MIN)

data access:
4tCLK - t29(82288-8)MAX - tD(IC21/22)MAX - t8(80286)MIN =
= 250 - 20 - 20 - 10 = 200 ns < 160 ns (tRLDV 8259A-2)

write cycle:

tWLWH (write):
4tCLK - t29(82288-8)MAX + t30(82288-8)MIN =
= 250 - 20 + 5 = 235(min) < 190 ns (tWLWH 8259A-2)

tAHWL (CS-/A0 to write):
7tCLK - t16(82288-8)MAX - tD(IC23/24)MAX = t29(82288-8)MIN =
= 375 - 15 - 20 + 3 = 343 > 0 (tAHWL MIN)

data setup time:
8tCLK - tD(IC30)MAX - t26(82288-8)MAX - tD(IC21/22)MAX =
= 500 - 10 - 25 - 20 = 445 ns > 160 us (tDVWH 8259A-2)

4. RTC cycle worst case (MC 146818)

All times tX are related to Motorola MC146818 timming data.

t1: 16tCLK - t16(82288-8)MAX - tD(IC30)MAX =
= 1000 - 15 - 10 = 975 > 953 ns (MIN)

t2: 8tCLK - t29(82288-8)MAX + t30(82288-8)MIN =
= 500 - 20 + 3 = 483 > 300 (MIN)

t3: 6tCLK - t30(82288-8)MAX + t29(82288-8)MIN =
= 375 - 20 + 3 = 358 > 325 (MIN)

t24: 2tCLK - t16(82288-8)MAX - tD(IC23/24)MAX - tD(IC25)MAX +
+ tD(IC30)MIN = 125 - 15 - 20 - 30 + 0 + 60 > 50 (MIN)

t25: tCLK - tD(IC30)MAX + tHOLD(IC25)MIN =
= 62,5 - 10 + 0 = 52,5 > 20 (MIN)

read access time:
6tCLK - t29(82288-8)MAX - t30(MC146818)MAX - t8(80286-8)MIN=
= 375 - 20 - 240 - 10 = 105 > 0

write data setup time: more than enough.

5. NPX cycle worst case

All times tXXX are related to Intel 80287-3 timming data.

tAVRL, tAVWL:

7tCLK - t16(82288-8)MAX - tD(IC23/24)MAX + t30(82288-8)MIN =
= 437,5 - 15 - 20 + 3 = 405,5 ns > 0

tRLRH, tWLWH:

2tCLK - t29(82288-8)MAX + t30(82288-8)MIN =
= 125 - 20 + 3 = 108 ns > 95 ns

tRHAX, tWHAX:

tCLK - t30(82288)MAX + t16(82288-8)MIN + tD(IC23/24)MIN =
= 625 - 20 + 3 + 0 = 45,5 > 0

read data access time: garanted by 80286-8 and 80287-3 (80287-8) timings

write data setup time: garanted by 80286-8 and 80287-3 (80287-8) timings.

6. DRAM 8207 controller worst case timing

All times tX are related to Intel 8207-16 timming data.

Read cycle: (80286-8, 50256-12)

8207-16 t12: 2tCLK - t13(80286-8)MAX - tD(IC14,IC60)MAX -
- tD(IC66)MAX = 125 - 60 - 25 - 10 ns > 20 ns

8207-16 t13: 80286-8 ensures this time

D0 - D 15 CPU setup time:

3tCLK - t26(8207-16)MAX - tRAC(50256-12)MAX -
- (tRCD - tRCDMAX)MAX - tD(IC42/43)MAX - tD(IC40/41)MAX
- t8(80286-8)MIN = 187,5 - 35 - 120 - 2,5 - 8 - 10 - 10=
= 2 ns > 0

all DRAM timing parameters are garanted by 8207-16 for 50256-12 DRAMs.
In the case of back-to back memory cycles 8207-16 starts second memory cycle one clock later (adds one wait sttate) and satisfies DRAM tRP.

Write cycle: (80286-8, 50256-12)

8207-16 t12,t13: same as for read cycle

50256-12 DI setup time:

1tCLK - t14(80286-8)MAX - tD(IC40/41)MAX + t36(8207-16)
MIN + tD(IC75)MIN + tD(IC70)MIN =
= 62,5 - 50 - 10 + 0 + 0 + 0 =2,5 ns > 0

50256-12 DI hold time:

1tCLK - t36(8207-16)MAX + t36(8207-16)MIN + tD(IC39)MIN =
= 62,5 - 35 + 0 + 0 = 27,5 ns > 20 ns

All DRAM timing parameters are garanted by 8207-16 for 50256-12 DRAMs.
In the case of back-to back memory cycles 8207-16 inserts additional wait states to satisfy DRAMS RAS inactive time.

Refresh cycles timings and frequency are garanted by 8207-16.

7. VME bus master DTB timing worst case

DTB master timing is the same for write cycle followed by Read Cycle for Read Cycle followed by Write Cycle and for Interrupt acknowledge cycle.
All times tX are related to VMEbus Specification manual timming data.

Read cycle:

t1: 3tCLK - tD(IC13+IC18)MAX - tD(IC50/51/46/52)MAX =
= 187,5 - 20 - 25 = 142,5 > 35 ns

t2: MIN 2tCLK = 125 ns > 0

t3: 2tCLK - t30(82288-8)MAX = 125 - 20 = 105 > 40 ns

t4: MIN 2tCLK = 125 ns > 0

t5: = 0

t6: 3tCLK - tD(IC64) = 187,5 - 10 = 177,5 > 35 ns

t7: tD(IC64)tip = 10 ns

t8: 2tCLK - t30(82288-8)MAX = 125 - 20 = 105 > 0

t9: = 0

t10: MIN 2tCLK = 125 ns > 0

t11: 2tCLK - t30(82288-8)MAX - tD(IC12+IC66+IC64)MAX =
= 125 - 20 - 40 = 65 > 40

t12: 2 tCLK - t30(82288-8)MAX - tD(IC12+IC66+IC64)MAX =
= 125 - 20 - 40 = 65 > 40

t13: 2tCLK - t30(82288-8)MAX - tD(IC12+IC66+IC64)MAX =
= 125 - 20 - 40 = 65 > 40

t14: MIN 2tCLK = 125 > 0

t16: 2tCLK - t30(82288-8)MAX - tD(IC12+IC66+IC64)MAX =
= 125 - 20 - 40 = 65 > 40

CPU read data setup time:
2tCLK - t8(80286-8)MIN - tD(IC44/45)MAX - tD(IC40/41)MAX =
= 125 - 10 - 20 - 20 = 75 > 0

Write cycle

t1: same as for Read
t2: "
t3: "
t4: "
t5: same as for Read
t6: "
t7: "
t8: 2tCLK - t30(82288-8)MAX - tD(IC12+IC66+IC64)MAX =
= 125 - 20 - 40 = 65 > 0
t9: 3tCLK - tD(IC40/41)MAX - tD(IC44/45)MAX - tD(IC13+IC18)MAX -
- t28(82288-8)MAX =
= 187,5 - 20 - 20 - 20 - 30 = 97,5 > 35
t10: MIN 2tCLK = 125 > 0
t11: = 0
t12: MIN 2tCLK = 125 > 0
t13: 2tCLK - t30(82288-8)MAX - tD(IC12+IC66+IC64)MAX =
= 125 - 20 - 40 = 65 > 40
t14: same as t12 read cycle
t15: 2tCLK - t30(82288-8)MAX - tD(IC12+IC64+IC66)MAX =
= 125 - 20 - 40 = 65 > 40
t17: MIN 2tCLK = 125 > 0

Interrupt acknowledge cycle

t1: same as for read cycle
t2: "
t3: "
t4: "
t5: "
t6: "
t7: "
t10: "
t11: "
t13: "
t14: same as for t12 Read cycle

CPU read data setup time: same as for read cycle.

8. VME DTB slave timing worst case

All times tX are related to Intel 8207-16 timming data and to VMEbus Specefication Manual timming data.

8207-16 asinchronous mode timing (for read cycle and write cycle):

t17: garanted by VME DTB master (t5)
t16: min 4tCLK = 250 ns > 150 ns (t18 also)
t23: min 2tCLK = 125 ns > 35 ns
t24: min 2tCLK = 125 ns > 0

DTB slave read timing:

t15: min 1tCLK = 62,5 > 0
t16: 3tCLK - tRAC(50256-12)MAX - tD(IC42/43)MAX - tD(44/45)MAX -
- t26(8207-16)MAX =
= 187,5 - 120 - 10 - 10 - 35 = 12,5 > 0
t18: tD(IC39)MIN + tD(IC44/45)MIN = 0

t20: t38(8207-16)MIN = 0

Write cycle

50256-12 DI setup time:

2tCLK - t53(8207-16)MAX - tD(IC39) - tD(IC44/45) =
= 125 - 70 - 25 - 20 = 10 ns > 0

50256-12 DI hold time:

tCLK - t36(8207-16)MAX - tD(IC75+IC70)MAX =
= 62,5 - 35 - 7 = 20,5 > 20 ns

t15: min 4tCLK = 250 ns > 30 ns

t17: t38(8207-16)MIN = 0

12. VME CPU/286 RESIDENT FIRMWARE

VME CPU/286 board contains two 27256 EPROMs in which the resident firmware reside. There are VME CPU/286 Self Test, VME CPU/286 Monitor and VME CPU/286 Boot Loader that invokes XENIX V Operating System.

Power-on or hardware reset activates the VME CPU/286 Self Test. After successful completion of self test the default boot loader is automatically invoked (auto boot).

All self test messages are displayed on system console which is connected to RS232C serial communication port of VME CPU/286 board (Connector 'J2' on front panel of the board). The operator can always abort the self test with one of following commands:

<ctrl X> - abort self test and invoke VME CPU/286 Monitor

<any other key> - abort self test and invoke VME CPU/286 Boot Loader

'Trident' computer systems, in which IDC GRAF module and graphic terminal are installed, displayed self test messages on graphic terminal too. The operater can always abort the self test by pressing on any key on graphic terminal and invoke VME CPU/286 Boot Loader.

VME CPU/286 Boot Loader is operable on system console and on graphic terminal if it exists.

NOTE:

VME CPU/286 Monitor is operable only on system console!

12.1 VME CPU/286 SELF TEST V1.0

12.1.1 Introduction

The self test is used to verify the general operation of the VME CPU/286 board. The self test is automatically invoked each time ac power is applied to the system (power-up) or when the hardware RESET switch is pressed. The self test can run in normal or in repeat mode.

The following message should be displayed on system console and on graphic terminal if it exists, upon successful completion of self test by normal mode (approx. 35sec.).

VME CPU/286 Self Test Vx.y

PASSED

where 'x.y' is the release level.

Error messages have on system console the following form

name parameters FAILED

where 'name' is name of test sequence and 'parameters' if they exist, are pointers to detected error.

On graphic terminal in case the error was detected only message 'FAILED' is displayed, without error descriptions.

The self test runs in repeat mode when repeat flag in table of parameters is set. After each completion of self test in this mode message 'PASSED' is replaced with current time from real time clock.

The self test can display on the start of each test sequence its serial number and can execute short or long version of RAM test, depends of the flags in table of parameters.

The self test is executed by power-on or by hardware reset in normal mode with short version of RAM test and no sequence number is displayed. If the self test is invoked by VME CPU/286 Monitor, the repeat mode, long version of RAM test and sequence number displaying are set.

Simple status information of self test are displayed on status leds of VME CPU/286 board too.

12.1.2 Description

VME CPU/286 Self Test is divided into more test sequences. Following test sequences are executed without use of stack pointer and RAM. They are presented in the order in which they are executed. In brackets are serial numbers of test sequences.

Initialization 1 - Initializes iAPX 286 segment registers, loads interrupt descriptor table register (interrupt descriptor table is in ROM; interrupt vectors point to interrupt service routine which displays interrupt number and contents of all iAPX 286 registers), initializes real time clock (RTC), serial communication controller (SCC) and programmable interrupt controller (PIC).

(01) **Real Time Clock Test 1** - Verifies operation of periodic interrupt flag in status register C of RTC.

(02) **Serial Communications Controller Test 1** - Verifies the contents off all status registers of channel A.

(02) **Serial Communications Controller Test 2** - Verifies the contents off all status registers of channel B.

(02) **Serial Communications Controller Test 3** - Writes two characters to data register A and verifies if transmit register empty flag in status register A is cleared.

(02) **Serial Communications Controller Test 4** - Verifies if transmit register empty flag in status register A is set after 1.4 msec. after writing data in data register A.

(03) **Programmable Interrupt Controller Test 1** - Verifies operation of interrupt 0 flag in interrupt request register of PIC. Interrupt 0 is connected with SQW output of RTC.

(04) **ROM Test 1** - Checks ROM begin and end address from table of parameters. ROM test 2 is skipped if begin address is equal to end address.

(05) **ROM Test 2** - Calculates check word (CRC) for ROM area and compares it with reference code in table of parameters. Calculated check word is displayed on CRT screen if check words not match.

(06) **RAM Test 1** - Checks RAM begin and end address from table of parameters. RAM test 2 is skipped if begin address is equal to end address.

(07-27) **RAM Test 2** - Tests RAM area with 21 subsequences. If RAM

error is detected address of error location, expected pattern and error data are displayed on CRT screen.

Next test sequences run use the RAM. They are also presented in the order in which they are executed.

Initialization 2 - Initializes stack segment and stack pointer, copies interrupt descriptor table to RAM and loads interrupt descriptor table register.

(30) **Programmable Interrupt Controller Test 2** - Enables tick interrupt and verifies if interrupt is generated. Interrupt vector is sent from PIC.

(31) **Bus Time Out Test 1** - Loads contents of not present port (on address 0100h) and verifies if NMI interrupt is generated.

(31) **Bus Time Out Test 2** - Verifies states of flags in status register after service of non-maskable interrupt.

(32) **Real Time Clock Test 2** - Verifies operation of UIP flag in status register A of RTC.

(33) **Real Time Clock Test 3** - Set alarm registers (real time + one second), enables alarm interrupt and verifies if alarm interrupt is generated. Interrupt vector is sent from PIC.

(34) **Serial Communications Controller Test 5** - Enables Tx interrupt of SCC and verifies if interrupt is generated. Interrupt vector is sent from PIC.

(35) **Serial Communications Controller Test 6** - Enables Tx interrupt of SCC and verifies if interrupt is generated. Interrupt vector is sent from SCC.

(36) **Numeric Processor Extension Test 1** - Verifies status word of NPX after initialization.

(36) **Numeric Processor Extension Test 2** - Initializes all NPX registers, executes numeric operations and compares contents of NPX registers with values from reference table. If contents do not match then offset to the reference table, value from the table and NPX register value are displayed.

(37) **Serial Communications Controller Test 7** - Verifies receive register full flag in status register B. If flag is permanently set after data read from data register B, error message is displayed.

(37) **Serial Communications Controller Test 8** - Verifies transmit register empty flag in status register B. If

flag is permanently clear, error message is displayed.

(37) **Serial Communications Controller Test 9** - This test sequence requires connection between Rx and Tx pin (pins 2 and 3) on connector J3 on front panel of VME CPU/286 board, and verifies transmition and reception of channel B. If pins aren't connected, test is skipped. In normal mode no error message is displayed.

(40-6Q) **VME Interface Test** - Initializes DMA controller on WDFD board and executes DMA transfer and CPU transfer between two memory segments parallel in the same time to test VME bus requester, VME bus arbiter, DTB operation and VME bus slave operation. VME Interface Test require DRAM 2MB memory board begin on 080000h address and WDFD board with DMA controller installed in system. Test is skipped if these boards are not installed (see chapter 16.1.7).

Upon successful completion of self test in normal mode the message 'PASSED' is displayed on system console and on graphic terminal if it exists and default boot loader is started (auto boot). In repeat mode the current time from RTC is displayed only on system console and the self test is repeated.

If any error is detected the execution of self test is terminated. Error message is displayed on system console, message 'FAILED' is displayed on graphic terminal and appropriate status information is sent to VME CPU/286 status leds.

The operator can always abort the self test on system console by pressing on 'ctrl X' key to start VME CPU/286 Monitor or by pressing on any other key to start VME CPU/286 Boot Loader.

On graphic terminal is allowed only start of VME CPU/286 Boot Loader by pressing on any key.

12.1.3 Messages on CRT Screen

no messages - No conditions for self test execution or SCC error, or communication with system console is in error, or system console is in error.

ABORTED - Self test was aborted by press on any key.

BTO1 FAILED - Non-maskable interrupt is not generated by bus time out error.

BTO2 FAILED - NMI status register mismatch after service of non-maskable interrupt.

DMA1 FAILED - DMA time out. No DMA transfer completion by VME interface test.

DMA2 FAILED - Error flag in channel status register of DMA controller is set after completion of data transfer by VME interface test.

NPX not present
- NPX status word error.

NPX2 oooo pp ee FAILED
- NPX register mismatch. 'oooo' - offset in NPX reference table, 'pp' - value from table, 'ee' - value of register.

PASSED -Self test completed; no errors (only in normal mode).

PIC1 FAILED - Interrupt 0 flag in interrupt request register of PIC does not update.

PIC2 FAILED - Tick interrupt (interrupt 40h) is not generated.

RAM1 FAILED - RAM begin segment or end segment address is not in form 0x000h, or end address < begin address.

RAM2 aaaa:aaaa pppp eeee FAILED
- Pattern 'pppp' and value 'eeee' of memory location 'aaaa:aaaa' mismatch. 'eeee' and 'pppp' may be the same values if the contents of memory location becomes right value during verifying and displaying.

ROM1 FAILED - ROM begin segment or end segment address is not in form 0x000h, or end address < begin address.

ROM2 cccc FAILED
- Check word mismatch. 'cccc' is new check word.

RTC1 FAILED - Periodic interrupt flag in interrupt request status of RTC does not update.

RTC2 FAILED - UIP flag in register A of RTC does not update.

RTC3 FAILED - RTC alarm interrupt (interrupt 41h) is not generated.

SCC1 FAILED - SCC status registers of channel A mismatch.

SCC2 FAILED - SCC status registers of channel B mismatch.

SCC3 FAILED - Transmit register empty flag in status register A of SCC is not cleared immediately after writing data in data register A.

SCC4 FAILED - Transmit register empty flag in status register A is not yet set after 1.4ms after writing data in data register.

SCC5 FAILED - SCC transmit register empty interrupt A (interrupt 41h) is not generated - interrupt vector is sent from PIC.

SCC6 FAILED - SCC transmit register empty interrupt A (interrupt 50h) is not generated - interrupt vector is sent from SCC.

SCC7 FAILED - Receive register full flag in status register B is permanently set.

SCC8 FAILED - Transmit register empty flag in status register B is permanently cleared.

SCC9 FAILED - Transmit and receive character mismatch by channel B test.

SCCb skipped
- No conditions for channel B test. Tx and Rx pin are not connected. This message is displayed only in repeat mode.

Trap tt
DS SI ES DI SS SP BP DX CX BX AX CS IP FLAG
aaaaaaaa aaaaaaaa aaaaaaaa aaaa aaaa aaaa aaaa aaaa aaaaaaaa aaaa

- Not expected trap or interrupt no. 'tt' is generated. 'aaaa' are values of iAPX 286 registers before execution of trap/interrupt service routine. These values are not valid if the stack RAM is not o.k.

VME1 aaaa:aaaa dddd bbbb:bbbb eeee FAILED
- Error by DMA transfer or by CPU transfer or by CPU

verification. 'aaaa:aaaa' is source address, 'dddd' is source data, 'bbbb:bbbb' is destination address and 'eeee' is destination (error) data. 'dddd' and 'eeee' may be the same values if the contents of memory location becomes right value during verifying and displaying.

VME skipped - No conditions for VME interface test execution. VME interface test require DRAM 2MB memory board and WDFD board with DMA controller installed in system (see chapter 16.1.7). This message is displayed only in repeat mode.

hh:mm:ss - Current time from RTC which is displayed after each completion of self test in repeat mode.

12.1.4 Status Informations on VME CPU/286 Leds

VME CPU/286 board has three status leds: red, yellow and green (HALT, INTERRUPT, RUN). These three leds are used by self test to sending follow status informations to operator:

red	yellow	green	STATUS
0	0	1	self test execution
0	8Hz	1	RAM test execution
0	1	1	RAM test delay (refresh test)
1	x	0	immediately after start - RTC error(RTC1)
1	x	0	1 sec. after start - PIC error (PIC1)
0	0	0	trap/interrupt error
0	.	1	SCC error (no message,SCC1,SCC2,SCC3,SCC4)
0	..	1	ROM error (ROM1,ROM2)
0	...	1	RAM error (RAM1,RAM2)
0	....	1	other errors (PIC2,RTC2,RTC3,BTO1,BTO2, SCC5-SCC9,NPX2,DMA1,DMA2,VME1)

0 - switched off
1 - switched on
x - undefined
8Hz - 8Hz clock on yellow led
. - one pulse on yellow led every two seconds
.. - two pulses on yellow led every two seconds
... - three pulses on yellow led every two seconds
.... - four pulses on yellow led every two seconds

All other status informations are not valid and that means that the execution of self test is irregular or the leds are not o.k.

12.1.6 Table of parameters

Table of parameters is placed on beginning of self test and contains following parameters:

NAME	OFFSET	DESCRIPTION
checkw	08003h	Check word (CRC) for ROM test
begofo	08005h	begin offset
begseo	08007h	begin segment(*)
endofo	08009h	end offset
endseo	0800bh	end segment(*)
begoff	0800dh	begin offset for RAM test
begseg	0800fh	begin segment(*)
endoff	08011h	end offset
endseg	08013h	end segment(*)
delay	08015h	delay for refresh test in sec.
optflg	08017h	option flags(**)

(*) Processor iAPX 286 operates in real address mode. The segment address should be in form 0x000h.

(**) option flags: D0 - repeat flag
D1 - display flag
D2 - RAM test flag
D3 - parallel display flag

repeat flag: 0 - normal mode
1 - repeat mode

display flag: 0 - no sequence number displaying
1 - sequence number displaying on start of each sequence

RAM test flag: 0 - long version of RAM test
1 - short version of RAM test

Parallel display flag: 0 - messages are displayed only on system console (via RS232C)
1 - messages are displayed on system console and on graphic terminal if IDC GRAF module is installed

NAME	OFFSET	DESCRIPTION
boot_dev	0ffffh	Boot Loader command (ASCII char) for auto boot

12.1.7 Hardware Configuration for VME Interface Test

VME interface test is intended to test VME bus requester, VME bus arbiter, DTB operation and VME bus slave operation. Test program initiates memory to memory data transfers at the same time. CPU checks data blocks was transferred correctly.

For running VME interface test program we need next HW configuration:

- VME CPU/286 under test
- WDFD controller board
- DRAM 2MB board

VME CPU/286 under test must be located in slot 1 of VME bus backplane. It must have next jumper settings:

JMP:	1 - 2	connected
	3 - 4	connected
JNPX:	2 - 5	connected
	3 - 4	connected
JEPR:	3 - 4	connected
IACK:	1 - 2	connected
JRC:	1 - 16	connected
	2 - 15	connected
	3 - 14	connected
	5 - 12	connected if 80286-8 (open if 80286-6)
	6 - 11	connected if 50256-12 (open if 50256-15)
	7 - 10	connected
JJ2:	7 - 16	connected
	9 - 16	connected
	10 - 16	connected
JJ3:	7 - 16	connected
	9 - 16	connected
	10 - 16	connected

WDFD board must be located in slot 2 of the VME bus backplane. DMA controller base address must be 0e300h in IO space (AM = 02dh). Board must generate interrupts on IRQ4* VME bus interrupt request line. Board must request bus on BR3* bus request line. There is no need for any jumper settings on the WDFD board.

DRAM 2MB must be located in slot 3 of the VME bus backplane. It must be mapped begin on 080000h address in memory address space (AM = 03dh). Jumpers must be set this way:

```
J2:     2 - 17   connected
        4 - 15   connected
        6 - 13   connected
        7 - 12   connected
        8 - 11   connected
        9 - 10   connected
J3:
J4:     5 -  8   connected
```

12.2 VME CPU/286 MONITOR V1.0

12.2.1 INTRODUCTION

The VME CPU/286 Monitor is started if the <ctrl X> key was pressed on system console during self test execution or in VME CPU/286 Boot Loader.

The following message should be displayed on system console immediately after start of VME CPU/286 Monitor

```
Hello !!!

VME CPU/286 Monitor Vx.y

$$$
```

where 'x.y' is the release level.

VME CPU/286 Monitor is operable only on system console.

The monitor works on both Intel iAPX 286 modes, in Real Addressing Mode (prompt is "$$$") and in Protected Virtual Addressing Mode (prompt is ">>>").

12.2.2 MONITOR COMMANDS

D - DUMP MEMORY BLOCK

Syntax: D S<selector>:C<start_offset> S<end_offset>C

Dump command displays a block of memory locations defined by selector, start and end offset. The displayed information is presented by hexadecimal values. If <selector> is not defined the last selector value is valid. If <end_offset> is not defined 256 bytes memory block is displayed.

Example:

```
$$$ d 1000:0000 001f<cr>
1000:0000 30 31 32 33 34 35 36 37 38 39 41 42 43 44 45 46  0123456789
1000:0010 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00  ..........
$$$
```

S - DISPLAY / SET MEMORY

Syntax: S S<selector>:C<offset>

With this command is possible to read/write to memory locations. After execution of set command the memory location and value is displayed. With additional commands the memory contents of the same or additional memory locations can be examined. This commands are:

<.> (dot)	return to monitor
</> (slash)	examine previous location || < > (space)	reexamine memory location
<cr> (carriage return)	examine next memory location
<hex byte cr>	write byte to memory location.

Example:

```
$$$ s 0000<cr>
1000:0000 30<cr>
1000:0001 31 40
1000:0002 32</>
1000:0001 40<.>
$$$
```

P - INPUT / OUTPUT TO PORT

Syntax: P S<byte_high>C<byte_low>

With Port command we can read/write to 8 bit or 16 bit port. After execution of Port command the port location and value is displayed. With additional commands the contents of the same or additional ports can be examined. This commands are:

<.> (dot)	return to monitor
</> (slash)	examine previous port || < > (space)	reexamine port
<cr> (carriage return)	examine next port
<hex byte/word cr>	write byte or word to port. Carriage return must be pressed.

Example:

```
$$$ P 00<cr>
0000 11<cr>
0001 00<.>
$$$
```

M - MOVE MEMORY BLOCK

Syntax: M S<sel_1>:C<start_off> <end_off> S<sel_2>:C<dest_off>

Move command copies a memory block (<sel_1>:<start_off> - <sel_1>:<end_off>) to specified memory block beginning on address <sel_2>:<dest_off>.

F - FILL MEMORY BLOCK WITH PATTERN AND VERIFY

Syntax: F S<selector>:C<start_off> <end_off> <word_pattern>

Fill command loads into defined block of memory a word pattern and verifies if the memory contents is valid. Word pattern is a four digit hexadecimal value. If contents is not valid the address and pattern is displayed.

V - VERIFY TWO MEMORY BLOCKS

Syntax: V S<sel_1>:C<start_off> <end_off> S<sel_2>:C<dest_off>

This command allows to compare if two memory blocks hold

identical values. If there is an error the addresses and values are displayed.

L - LOAD INTEL HEX FILE VIA AUXILIARY CHANNEL

Syntax: L S<selector>:C<offset>

With this command is possible to transfer file in Intel hexadecimal format from host computer to VME CPU/286 memory. The transfer is done via auxiliary serial port with 9600 baud speed (connector J3 on front panel of VME CPU/286 board).

Current selector and offset values are calculated with addition of <selector> / <offset> values and selector / offset values, which are defined in hex. format. Default <selector> value is 0000h, so we normal use command 'L 0000' to load file on addresses defined in hex. file (see appendix A).

Start address is also saved and we can start program after loading with 'R' command.

G - EXECUTE PROGRAM

Syntax: G S<selector>:C<offset>

Execute command transfers control to program which start address is defined in command.

R - RESTART PROGRAM

Syntax: R

With Restart command is possible to restart program execution from displayed value of CS and IP register. This is done by pressing carriage return <cr>. If the restart address is wrong we can start the program with command Go. Return to monitor is done with dot (.) command.

B - SET BREAKPOINT

Syntax: B S<selector>:C<offset>

With breakpoint we define address in program space where the

execution stops. At the breakpoint all 14 CPU registers are dumped on console, and control is transferred to monitor. After the breakpoint the execution continues by commands Trace or Intret.

Example:

```
$$$ b 1000:2003<cr>
$$$ g 1000:2000<cr>
addr code      DS   SI   ES   DI   SS   SP   BP   DX   CX   BX   AX   CS
2003 8ED8     00002000 00001000 0010FEBA DD39 2000 0000 D7C3 0000 1000
$$$
```

Examples of commands 'B' and 'T' are executed on follow sample program:

```
  1000                                cseg    1000h
                                      org     2000h
                            begin:
2000 B80000                           mov     ax,0
2003 8ED8                             mov     ds,ax
2005 B80020                           mov     ax,2000h
2008 8EC0                             mov     es,ax
200A B81030                           mov     ax,3010h
200D 8ED0                             mov     ss,ax
200F BC3433                           mov     sp,3334h
2012 BF4444                           mov     di,4444h
2015 BE5555                           mov     si,5555h
2018 BD6666                           mov     bp,6666h
201B BA7777                           mov     dx,7777h
201E B98888                           mov     cx,8888h
2021 BB9999                           mov     bx,09999h
2024 B8AAAA                           mov     ax,0aaaah
2027 2EC7063E203E                     mov     cs:laaa,offset laaa
     20
202E E80A00          203B             call    bbb
2031 90                               nop
2032 40                               inc     ax
2033 2EFF063E20                       inc     cs:laaa
2038 E9C5FF          2000             jmp     begin

203B D1E0                   bbb:      shl     ax,1
203D C3                               ret

203E                        laaa      rw      1
                                      end
```


Izdaja	1					List	Stran	J	K	Identifikacijska številka
Št. obvestila	M-017					70				33837044
IskraDelta proizvodnja računalniških sistemov in inženiring, p.o.						Arhiv		Namesto identifikacijske številke: 220670444		

Obr. 38

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T - TRACE PROGRAM

Syntax: T

With Trace command is possible to trace program after interrupt or breakpoint. It traces 10 program instructions and for each instruction displays offset, code and all 14 CPU registers.

Example:

```
$$$ t<cr>
addr code       DS   SI   ES   DI   SS   SP   BP   DX   CX   BX   AX
2005 B80020   00002000 00001000 0010FEBA DD39 2000 0000 D7C3 2000
2008 8EC0     00002000 20001000 0010FEBA DD39 2000 0000 D7C3 2000
200A B81030   00002000 20001000 0010FEBA DD39 2000 0000 D7C3 3010
200D 8ED0BC34 00002000 20001000 3010332E DD39 2000 0000 D7C3 3010
2012 BF4444   00002000 20004444 3010332E DD39 2000 0000 D7C3 3010
2015 BE5555   00002000 20004444 3010332E DD39 2000 0000 D7C3 3010
2018 BD6666   00002000 20004444 3010332E 6666 2000 0000 D7C3 3010
201B BA7777   00002000 20004444 3010332E 6666 7777 0000 D7C3 3010
201E B98888   00002000 20004444 3010332E 6666 7777 8888 D7C3 3010
2021 BB9999   00002000 20004444 3010332E 6666 7777 8888 9999 3010
$$$
```

```
 CS   IP   FLAG
10002008 0146
1000200A 0146
1000200D 0146
10002012 0146
10002015 0146
10002018 0146
1000201B 0146
1000201E 0146
10002021 0146
10002024 0146
```

I - RESTART EXECUTION AFTER INTERRUPT OR BREAKPOINT

Syntax: I

With Interrupt return command the execution of the program after any interrupt or breakpoint continues.

X - DISPLAY REGISTERS AFTER INTERRUPT OR BREAKPOINT

Syntax: X

This command displays all 14 CPU registers from stack after interrupt or breakpoint.

Example:

```
$$$ x<cr>
 DS   SI   ES  DI   SS  SP   BP   DX   CX   BX   AX   CS  IP  FLAG
00002000 20004444 3010332E 6666 7777 8888 9999 3010 10002024 0146
$$$
```

E - HARD MEMORY TEST

Syntax: E

This command tests defined 64Kbyte block of memory. The execution takes a lot of time. For each test cycle a "+" is displayed and for error cycle a "G" is displayed.

Y - FIND RAM

Syntax: Y

This command seeks in whole address space RAM and ROM areas. Physical start address, end address and type of areas are displayed.

Examples for Real and PVAM mode:

```
$$$ y<cr>                          >>> y<cr>
Real mode                          PVAM mode
000000-0effff RAM                  000000-27ffff RAM
0f0000-0fffff ROM                  ff0000-ffffff ROM
$$$                                >>>
```

Q - GO TO PVAM MODE

Syntax: Q

This command enters iAPX 286 into Protected Virtual Address Mode. It also displays Global descriptor Table, Interrupt Descriptor Table, Local Descriptor Table and Task Register. The monitor is now in PVAM mode and the PVAM prompt is displayed. All described monitor commands can be executed also in PVAM mode.

Example:

```
$$$ q<cr>
T 0000
G 002F FFFC90
I 008F FFFC00
L 0028
>>>
```

N - GO TO BOOT LOADER

Syntax: N

This command invoke VME CPU/286 Boot Loader to start Xenix V operating system. The command should be executed only in Real address mode (see chapter 16.3.1).

Z - GO TO SELF TEST

Syntax: Z

This command invoke VME CPU/286 Self Test with following options: repeat mode, long version of RAM test and sequence number displaying. The command should be executed only in Real mode.

12.2.3 MONITOR SELECTORS IN PROTECTED MODE

Global descriptor table (GDT) describes following selectors:

selector	memory area	type
0008	000000 - 00ffff	data
0010	010000 - 00fe00	stack
0018	ff0000 - ffffff	code
0020	000000 - 00ffff	code
0028	ffxxxx - ffxxxx	LDT

Local descriptor table (LDT) describes full 16M bytes address space with following selectors:

selector	memory area	type	selector	memory area	type
0004	000000 - 00ffff	data	0084	100000 - 10ffff	data
000c	010000 - 01ffff	data	008c	110000 - 11ffff	data
0014	020000 - 02ffff	data	0094	120000 - 12ffff	data
001c	030000 - 03ffff	data	009c	130000 - 13ffff	data
0024	040000 - 04ffff	data	00a4	140000 - 14ffff	data
002c	050000 - 05ffff	data	00ac	150000 - 15ffff	data
0034	060000 - 06ffff	data	00b4	160000 - 16ffff	data
003c	070000 - 07ffff	data	00bc	170000 - 17ffff	data
0044	080000 - 08ffff	data	00c4	180000 - 18ffff	data
004c	090000 - 09ffff	data	00cc	190000 - 19ffff	data
0054	0a0000 - 0affff	data	00d4	1a0000 - 1affff	data
005c	0b0000 - 0bffff	data	00dc	1b0000 - 1bffff	data
0064	0c0000 - 0cffff	data	00e4	1c0000 - 1cffff	data
006c	0d0000 - 0dffff	data	00ec	1d0000 - 1dffff	data
0074	0e0000 - 0effff	data	00f4	1e0000 - 1effff	data
007c	0f0000 - 0fffff	data	00fc	1f0000 - 1fffff	data
0104	200000 - 20ffff	data	0184	300000 - 30ffff	data
0204	400000 - 40ffff	data	0284	500000 - 50ffff	data
0304	600000 - 60ffff	data	0384	700000 - 70ffff	data
0404	800000 - 80ffff	data	0484	900000 - 90ffff	data
0504	a00000 - a0ffff	data	0584	b00000 - b0ffff	data
0604	c00000 - c0ffff	data	0684	d00000 - d0ffff	data
0704	e00000 - e0ffff	data	0784	f00000 - f0ffff	data

12.2.4 COMMAND SUMMARY

B - SET BREAKPOINT
B Š<selector>:Č<offset>

D - DUMP MEMORY BLOCK
D Š<selector>:Č<start_offset> Š<end_offset>Č

E - HARD MEMORY TEST
E

F - FILL MEMORY BLOCK WITH PATTERN AND VERIFY
F Š<selector>:Č<start_off> <end_off> <word_pattern>

G - EXECUTE PROGRAM
G Š<selector>:Č<offset>

I - RESTART EXECUTION AFTER INTERRUPT OR BREAKPOINT
I

L - LOAD INTEL HEX FILE VIA AUXILIARY CHANNEL
L Š<selector>:Č<offset>

M - MOVE MEMORY BLOCK
M Š<sel_1>:Č<start_off> <end_off> Š<sel_2>:Č<dest_off>

N - GO TO BOOT LOADER
N

P - INPUT / OUTPUT TO PORT
P Š<byte_high>Č<byte_low>

Q - GO TO PVAM MODE
Q

R - RESTART PROGRAM
R

S - DISPLAY / SET MEMORY
S Š<selector>:Č<offset>

T - TRACE PROGRAM
T

V - VERIFY TWO MEMORY BLOCKS
V Š<sel_1>:Č<start_off> <end_off> Š<sel_2>:Č<dest_off>

X - DISPLAY REGISTERS AFTER INTERRUPT OR BREAKPOINT
X

Y - FIND RAM
Y

Z - GO TO SELF TEST
Z

12.3 VME CPU/286 Boot Loader V1.0

12.3.1 Commands

'A' Load from winchester cylinder 0, head 1, sector 1 to memory location 3000:0000 and execute. Winchester must be formatted with 1024 bytes per sector and 8 sectors per track. ROM driver support FORCE SYS68K/WFC-1 winchester floppy controller.

'B' Load from floppy disk cylinder 1, head 0, sector 1 to memory location 3000:0000 and execute. Floppy disk with 48 TPI must be formatted with 1024 bytes per sector and 4 sectors per track. ROM driver support FORCE SYS68K/WFC-1 winchester floppy controller.

'W' Load from winchester cylinder 0, head 1, sector 1 to memory location 3000:0000 and execute. Winchester must be formatted with 512 bytes per sector and 16 sectors per track. ROM driver support IDC WDFD winchester floppy controller.

'F' Load from floppy disk cylinder 1, head 0, sector 1 to memory location 3000:0000 and execute. Floppy disk with 48 TPI must be formatted with 1024 bytes per sector and 4 sectors per track. ROM driver support IDC WDFD winchester floppy controller.

'ctrl X' - Go to VME CPU/286 Monitor.